

# 440LX CUSTOMER REFERENCE DESIGN

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Size  
A

Document Number  
Intel 440LX PCIsset

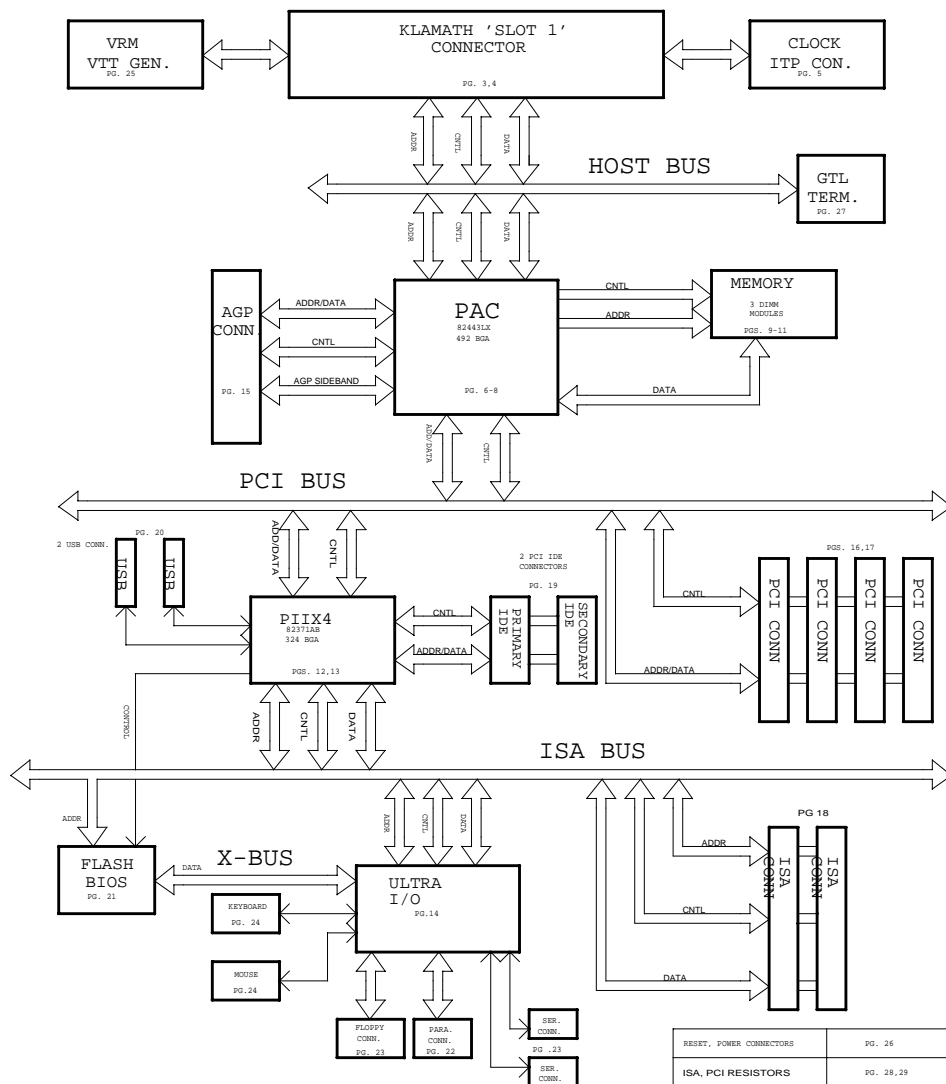
Rev  
1.4

Date:

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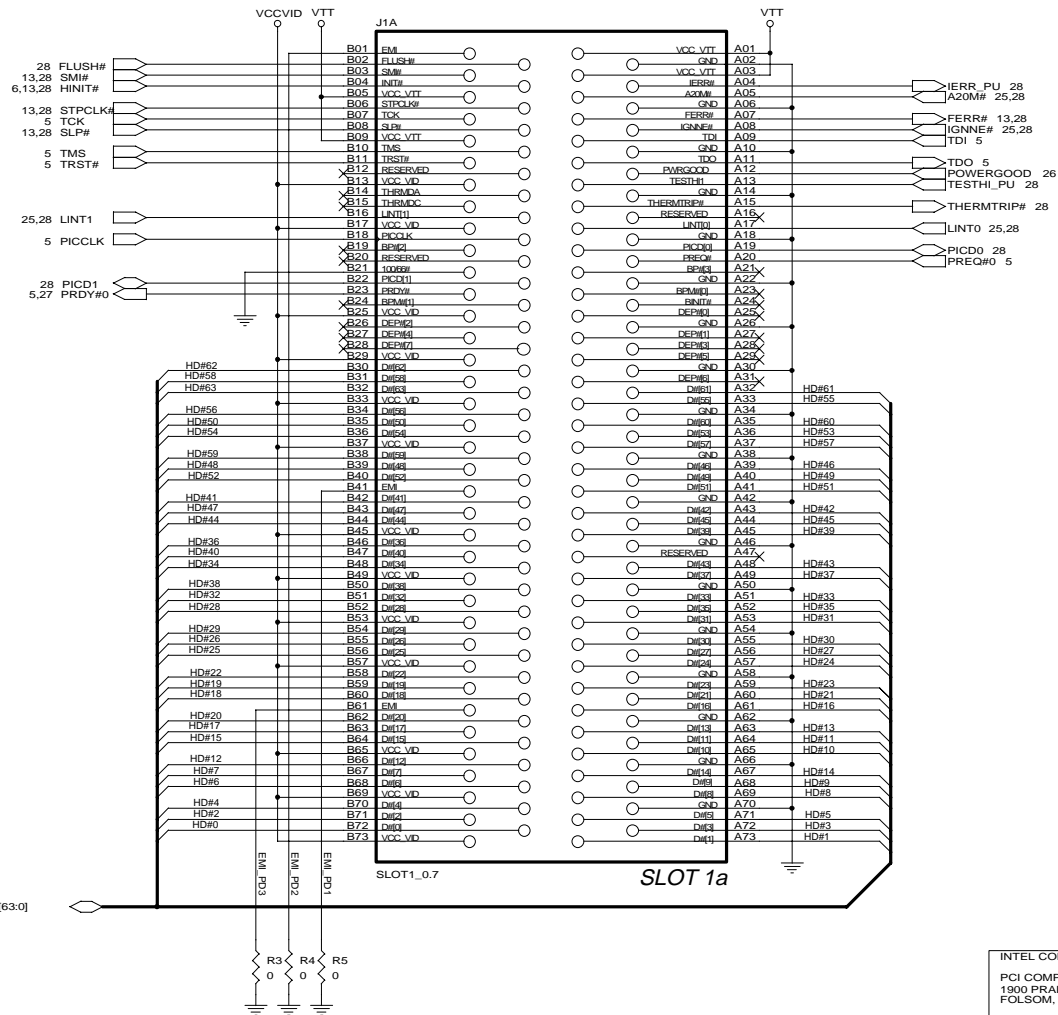
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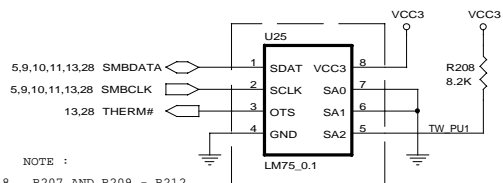
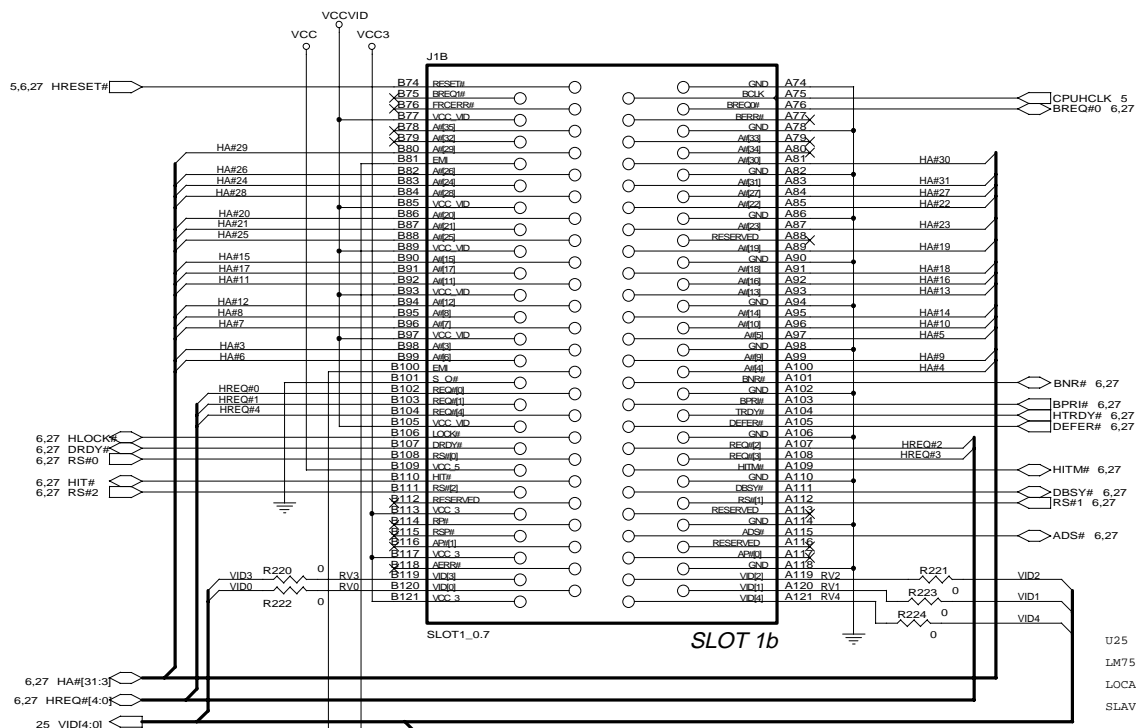
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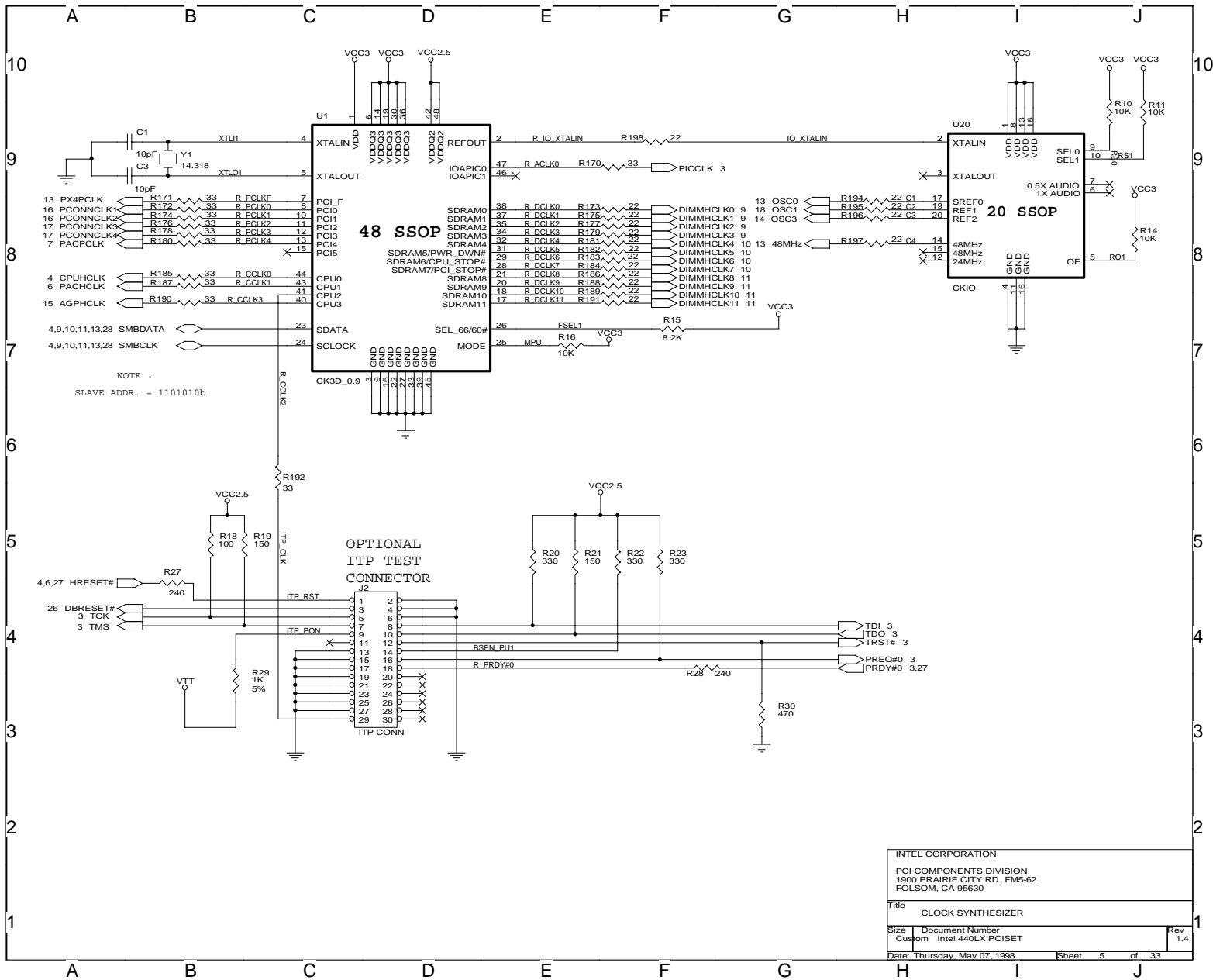
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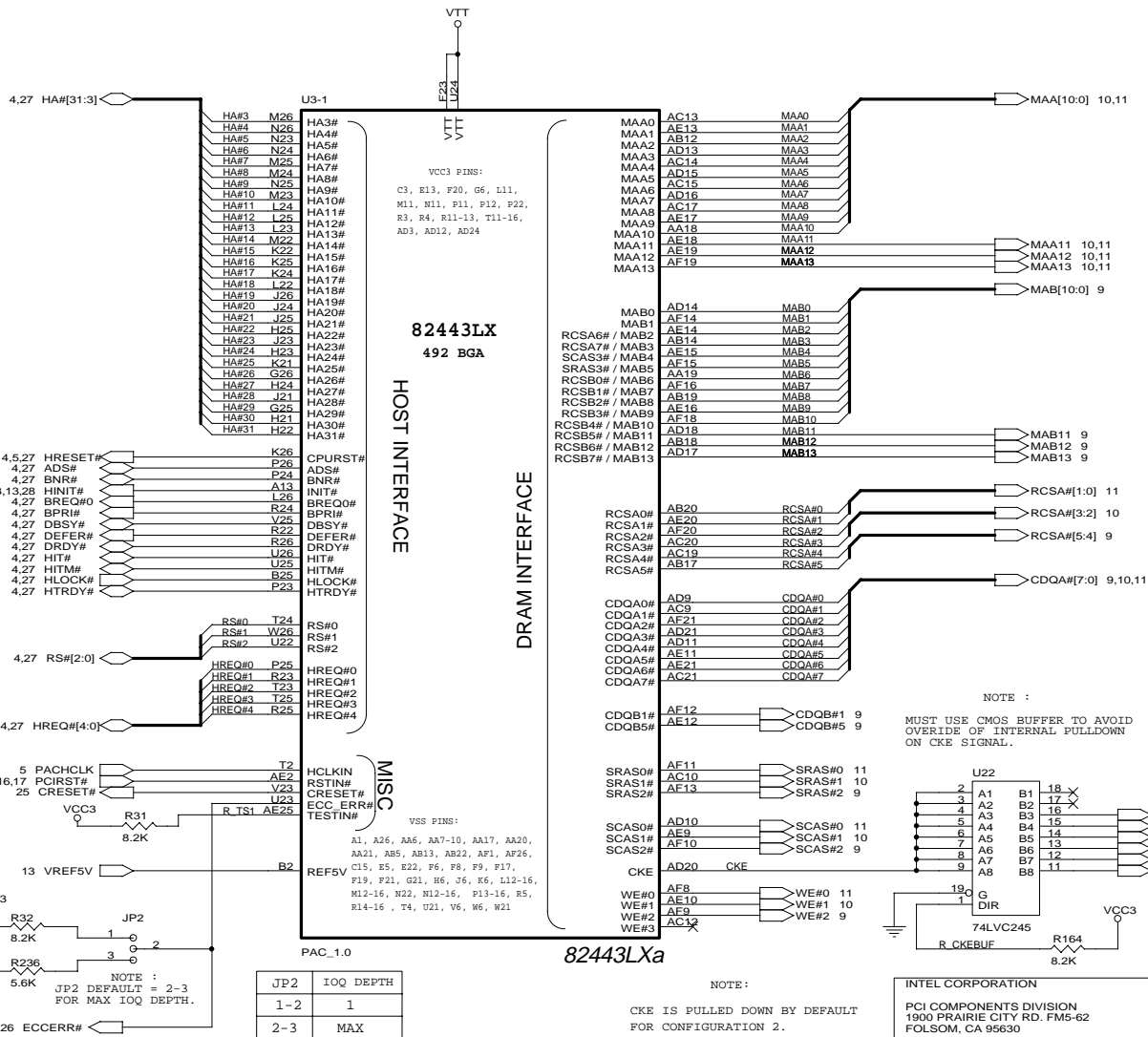
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Title SLOT 1 (PART II)		
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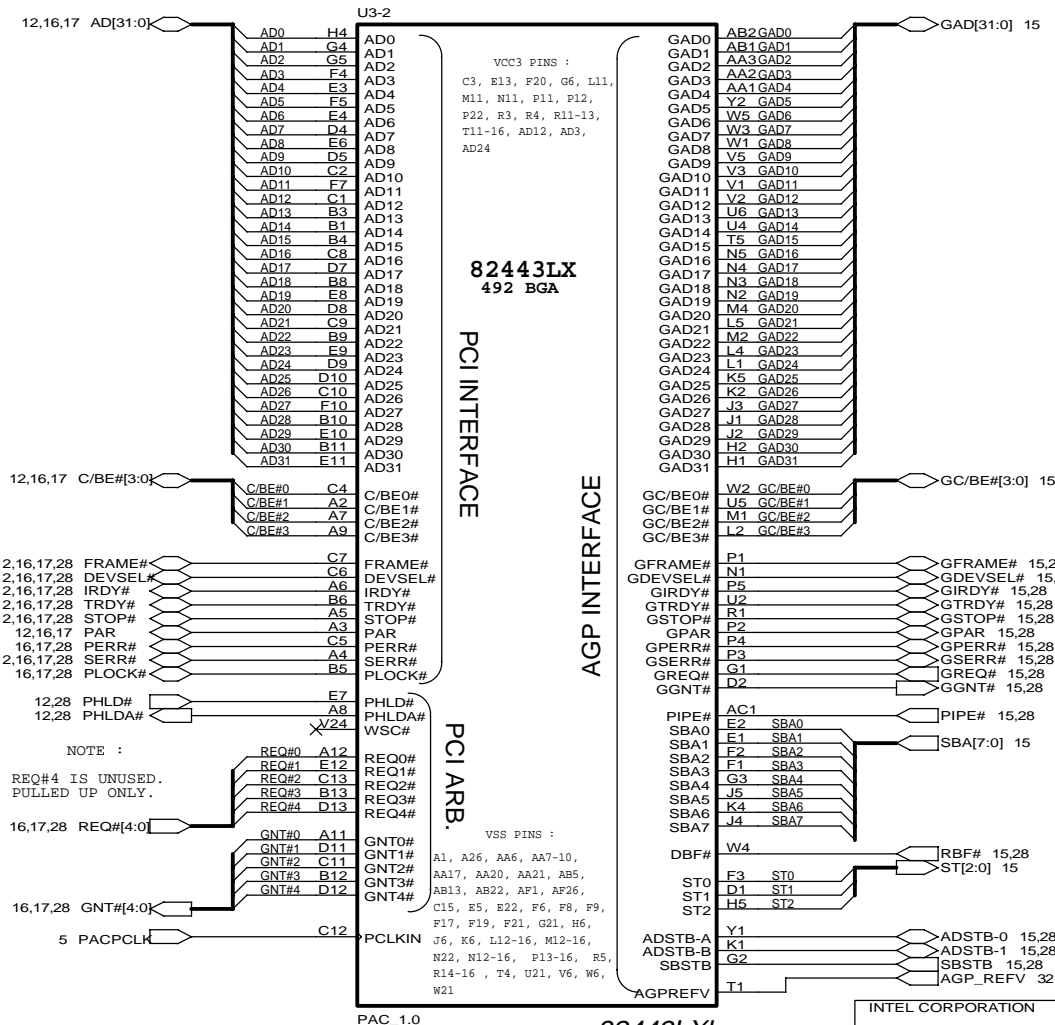


82443LXa

NOTE:

CKE IS PULLED DOWN BY DEFAULT  
FOR CONFIGURATION 2.  
SCHEMATICS WITH CONFIGURATION  
1 NEED A PULL-UP TO VCC3

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Title PAC HOST AND DRAM INTERFACES		
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9,10,11 MD[63:0]

U3-3

MD0	Y3	MD0
MD1	Y5	MD1
MD2	A5	MD2
MD3	AB4	MD3
MD4	AB6	MD4
MD5	AD1	MD5
MD6	AC5	MD6
MD7	AE1	MD7
MD8	AE3	MD8
MD9	AF3	MD9
MD10	AF4	MD10
MD11	AE5	MD11
MD12	AD6	MD12
MD13	AF6	MD13
MD14	AC7	MD14
MD15	AB8	MD15
MD16	AF23	MD16
MD17	AC22	MD17
MD18	AC23	MD18
MD19	AF25	MD19
MD20	AD25	MD20
MD21	AC24	MD21
MD22	AC26	MD22
MD23	AB23	MD23
MD24	AA22	MD24
MD25	AA24	MD25
MD26	AA25	MD26
MD27	Y22	MD27
MD28	Y24	MD28
MD29	Y25	MD29
MD30	W24	MD30
MD31	W25	MD31
MD32	AB3	MD32
MD33	AA4	MD33
MD34	AC2	MD34
MD35	Y6	MD35
MD36	AC4	MD36
MD37	AD2	MD37
MD38	AB7	MD38
MD39	AF2	MD39
MD40	AD4	MD40
MD41	AE4	MD41
MD42	AD5	MD42
MD43	AF5	MD43
MD44	AE6	MD44
MD45	AD7	MD45
MD46	AE7	MD46
MD47	AF7	MD47
MD48	AE23	MD48
MD49	AF24	MD49
MD50	AD23	MD50
MD51	AE26	MD51
MD52	AD26	MD52
MD53	AC25	MD53
MD54	AB24	MD54
MD55	AB25	MD55
MD56	AB26	MD56
MD57	Y21	MD57
MD58	AA26	MD58
MD59	W22	MD59
MD60	Y26	MD60
MD61	W23	MD61
MD62	V22	MD62
MD63	V21	MD63

VCC3 PINS :  
C3, E13, F20, G6,  
L11, M11, N11, P11,  
P12, P22, R3, R4,  
R11-13, T11-16, AD12,  
AD3, AD24

82443LX  
492 BGA

MEMORY DATA BUS

HOST DATA BUS

VSS PINS :  
A1, A26, AA6, AA7-10,  
AA17, AA20, AA21,  
AB5, AB13, AB22, AF1,  
AF26, C15, E5, E22,  
F6, F8, F9, F17, F19,  
F21, G21, H6, J6, K6,  
L12-16, M12-16, N22,  
N12-16, P13-16, R5,  
R14-16, T4, U21, V6,  
W6, W21

HD0#	G22	HD#0
HD1#	G23	HD#1
HD2#	F25	HD#2
HD3#	G24	HD#3
HD4#	F24	HD#4
HD5#	F26	HD#5
HD6#	E25	HD#6
HD7#	E24	HD#7
HD8#	F22	HD#8
HD9#	E26	HD#9
HD10#	D25	HD#10
HD11#	C25	HD#11
HD12#	D26	HD#12
HD13#	B26	HD#13
HD14#	E23	HD#14
HD15#	D24	HD#15
HD16#	B24	HD#16
HD17#	A26	HD#17
HD18#	A23	HD#18
HD19#	A22	HD#19
HD20#	A24	HD#20
HD21#	B23	HD#21
HD22#	B22	HD#22
HD23#	D23	HD#23
HD24#	D22	HD#24
HD25#	C22	HD#25
HD26#	B21	HD#26
HD27#	A21	HD#27
HD28#	D20	HD#28
HD29#	E21	HD#29
HD30#	D21	HD#30
HD31#	C21	HD#31
HD32#	F20	HD#32
HD33#	B20	HD#33
HD34#	A19	HD#34
HD35#	A20	HD#35
HD36#	B19	HD#36
HD37#	D19	HD#37
HD38#	C20	HD#38
HD39#	F18	HD#39
HD40#	E18	HD#40
HD41#	C18	HD#41
HD42#	D17	HD#42
HD43#	E19	HD#43
HD44#	C19	HD#44
HD45#	B18	HD#45
HD46#	B17	HD#46
HD47#	E17	HD#47
HD48#	C17	HD#48
HD49#	A17	HD#49
HD50#	B15	HD#50
HD51#	D16	HD#51
HD52#	D18	HD#52
HD53#	C16	HD#53
HD54#	E16	HD#54
HD55#	D15	HD#55
HD56#	A14	HD#56
HD57#	B16	HD#57
HD58#	C14	HD#58
HD59#	A16	HD#59
HD60#	A15	HD#60
HD61#	D14	HD#61
HD62#	E15	HD#62
HD63#	B14	HD#63

HD#[63:0] 3,27

9,10,11 MECC0  
9,10,11 MECC[7:1]

MECC0	AD8	MECC0
MECC1	AE8	MECC1
MECC2	AE22	MECC2
MECC3	AB21	MECC3
MECC4	AC8	MECC4
MECC5	AB9	MECC5
MECC6	AE22	MECC6
MECC7	AD22	MECC7

PAC\_1.0

82443LXc

GTL\_REF

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Size

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Intel 440LX PCISSET

1.4

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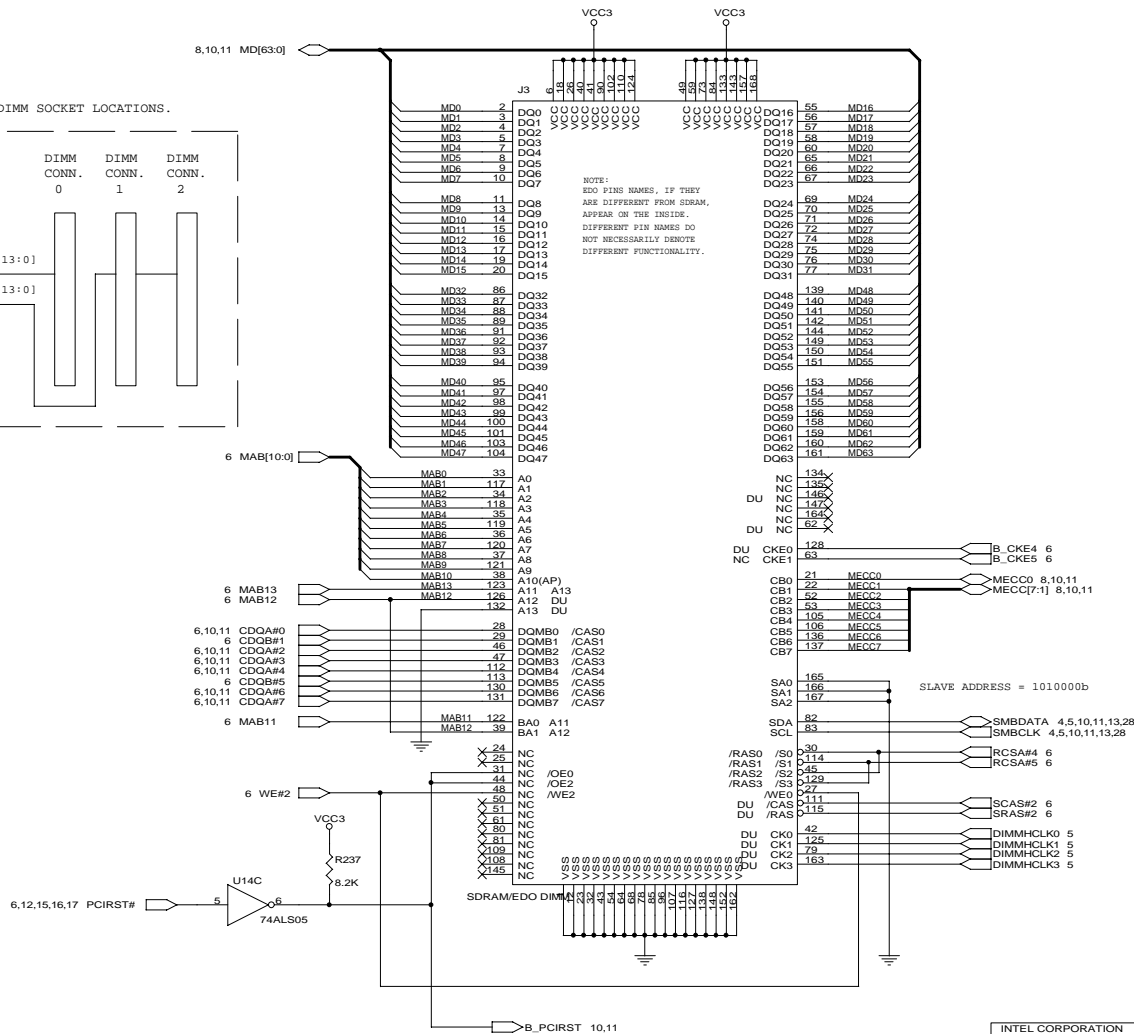
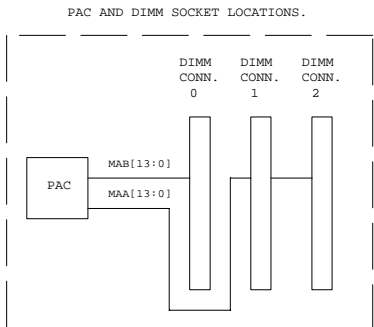
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of

33



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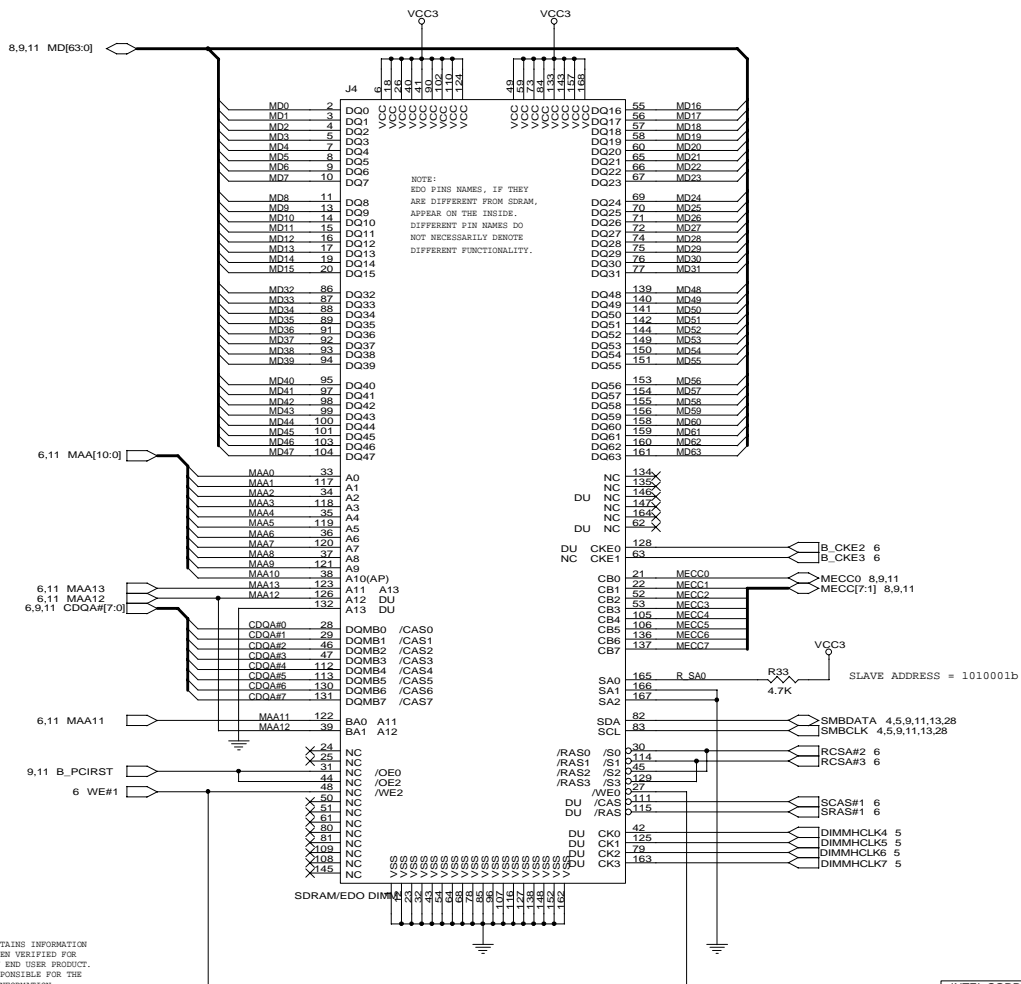


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Size	Document Number	Rev
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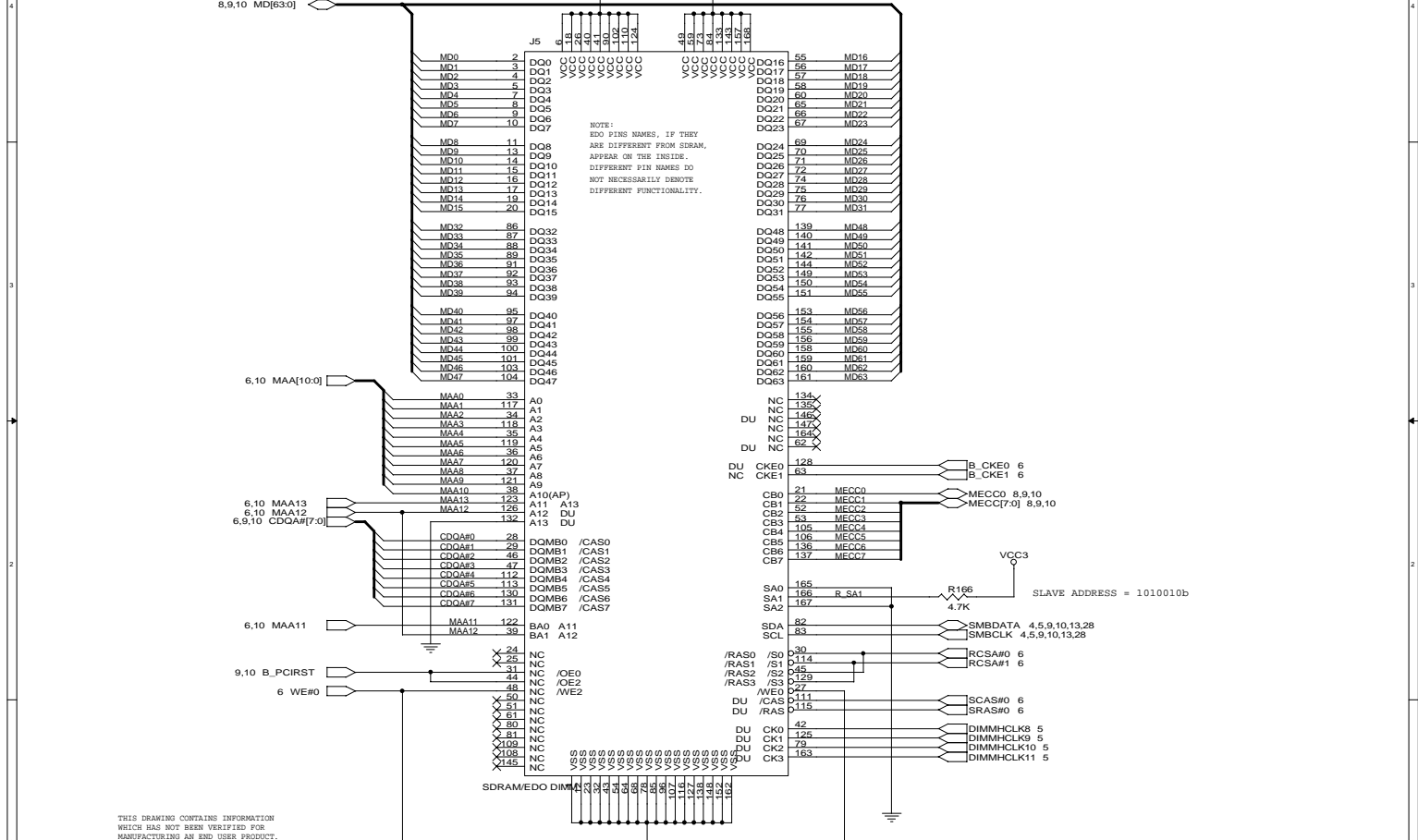


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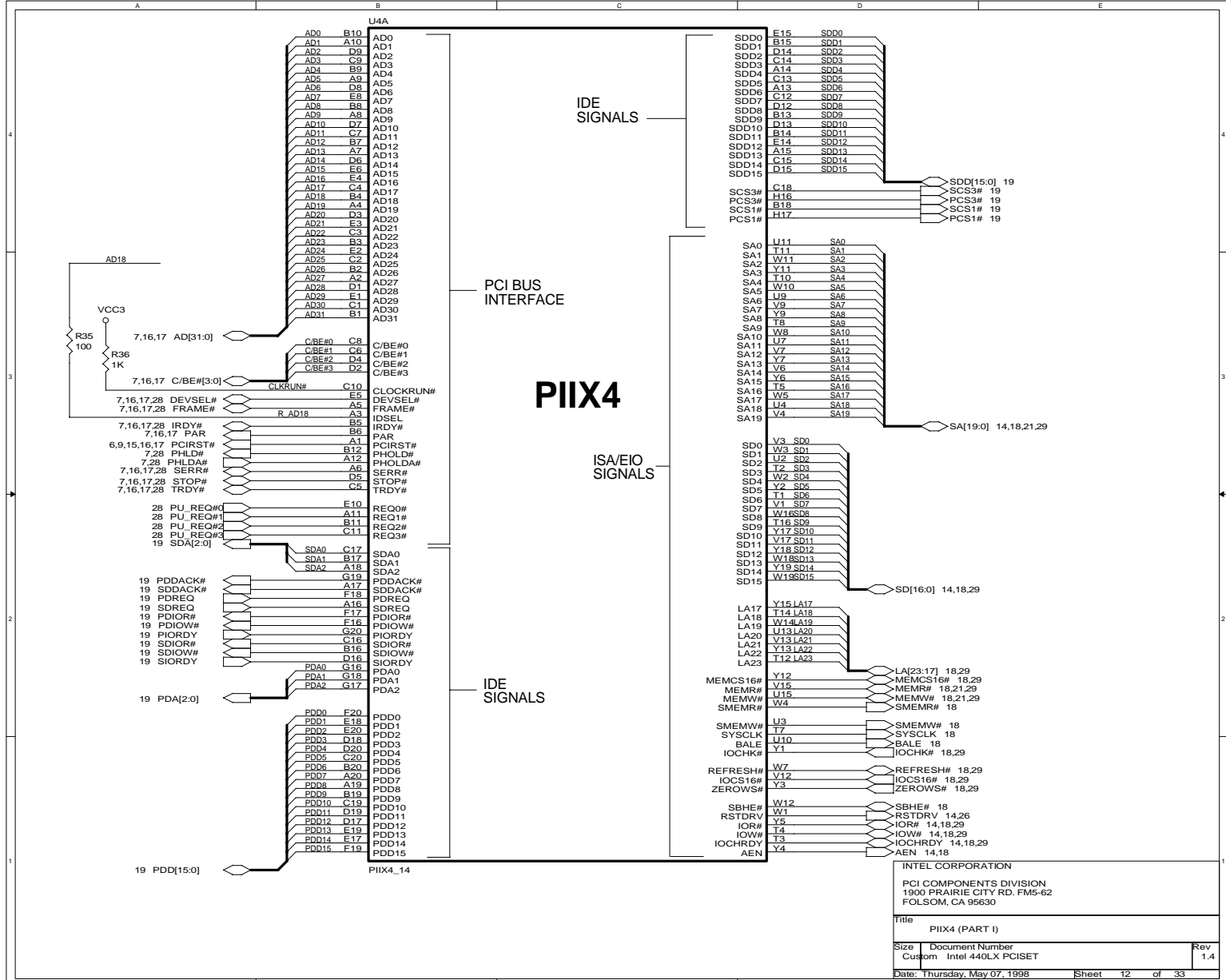
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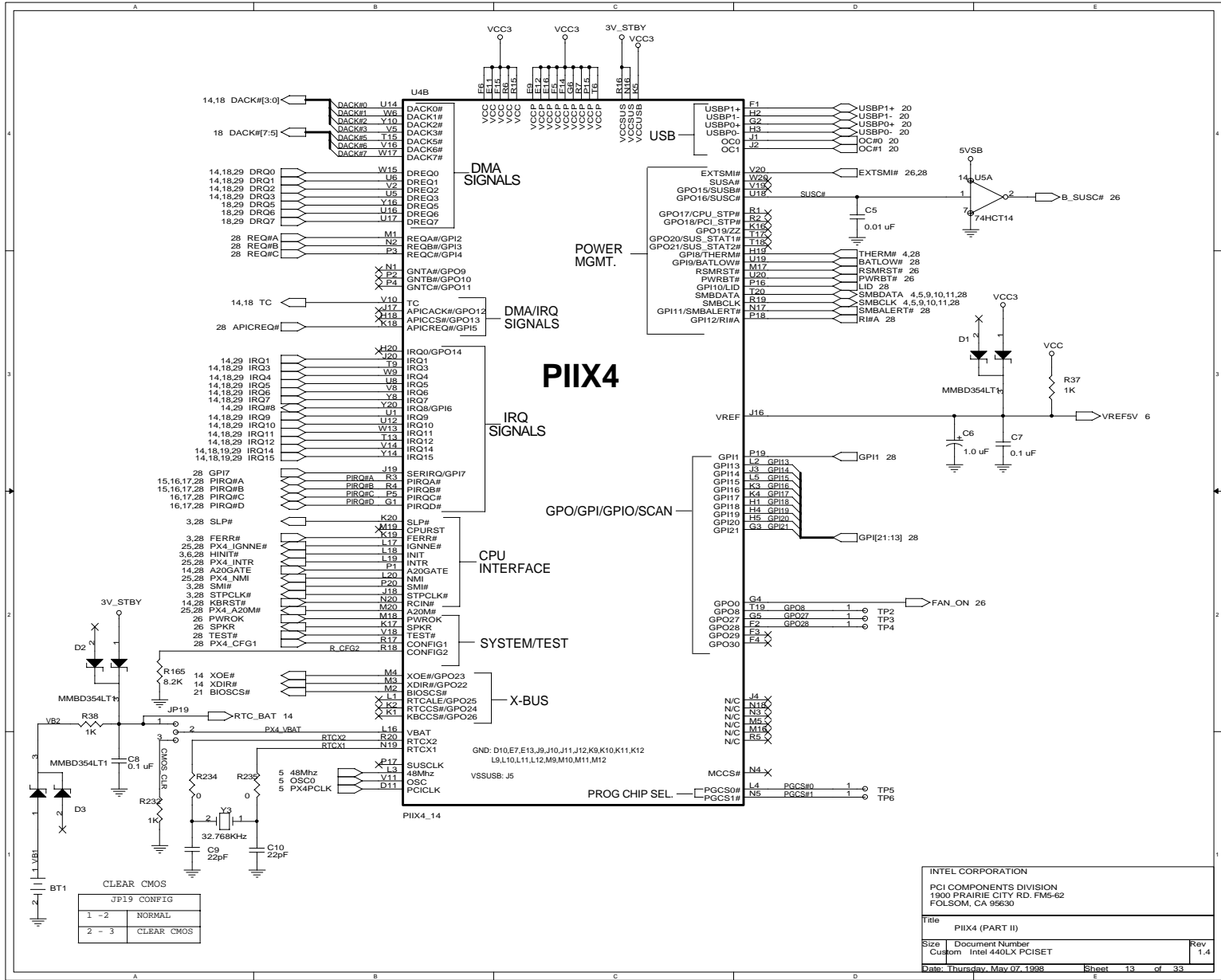
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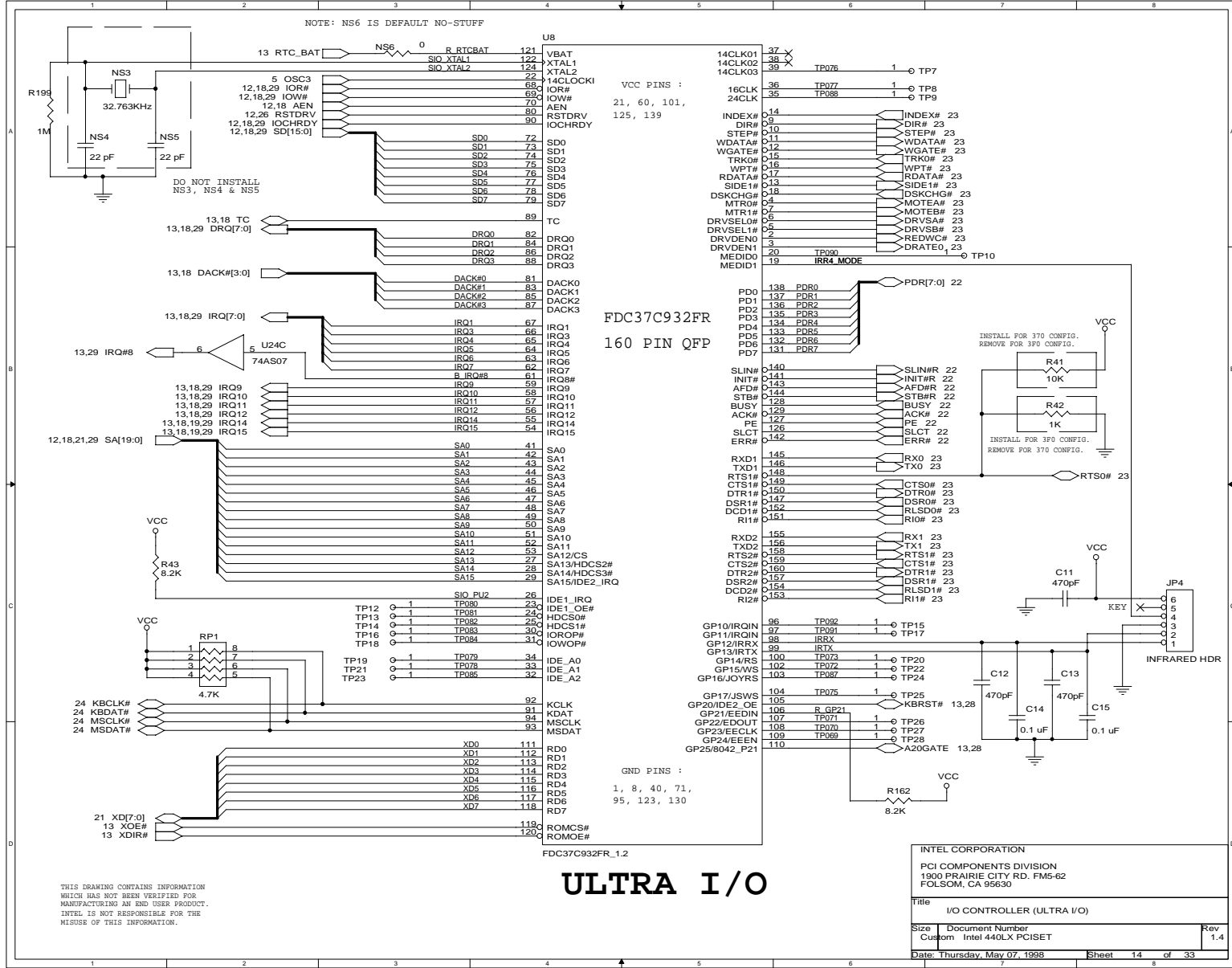


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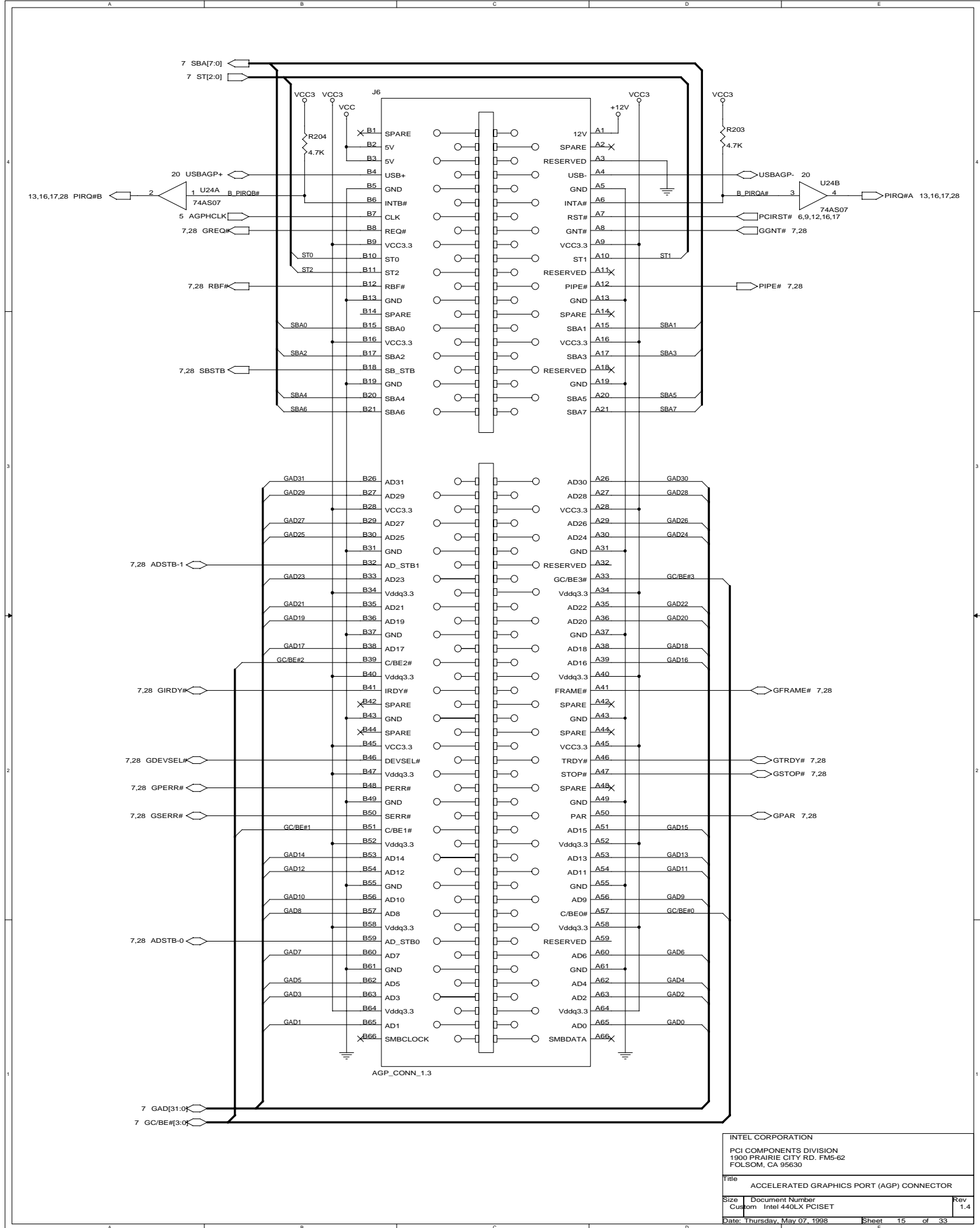
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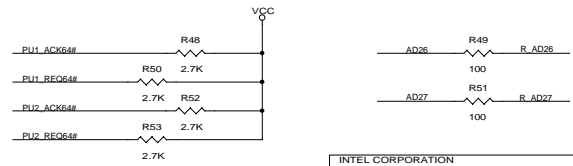
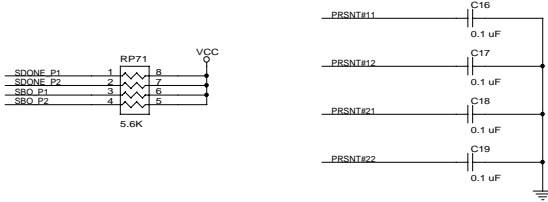
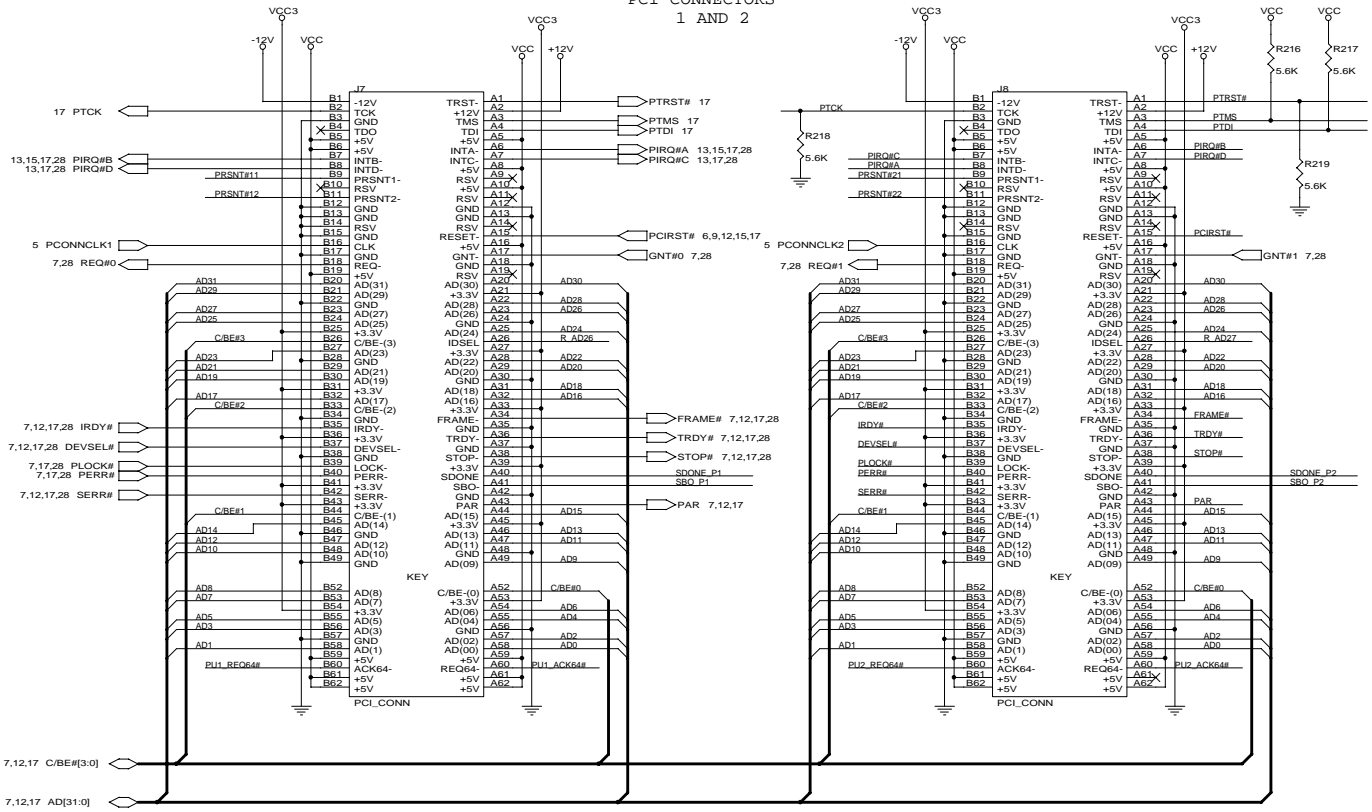




# ULTRA I/O



## PCI CONNECTORS 1 AND 2



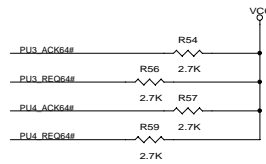
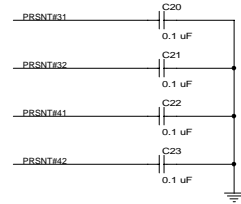
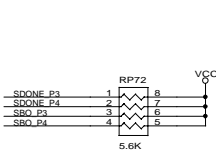
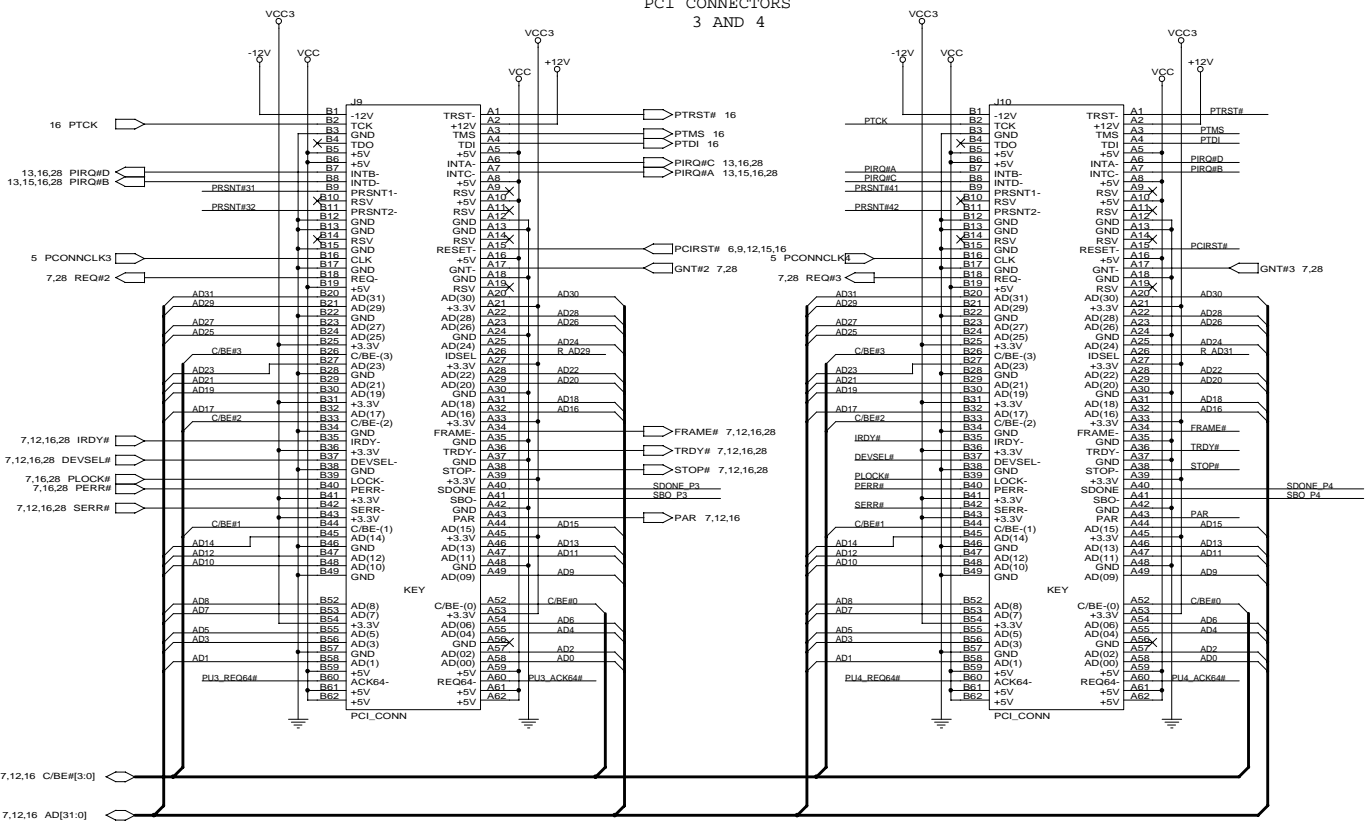
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PCI CONNECTORS  
3 AND 4

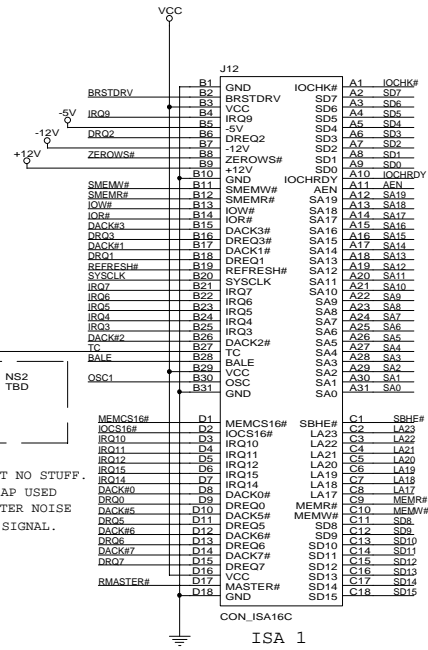
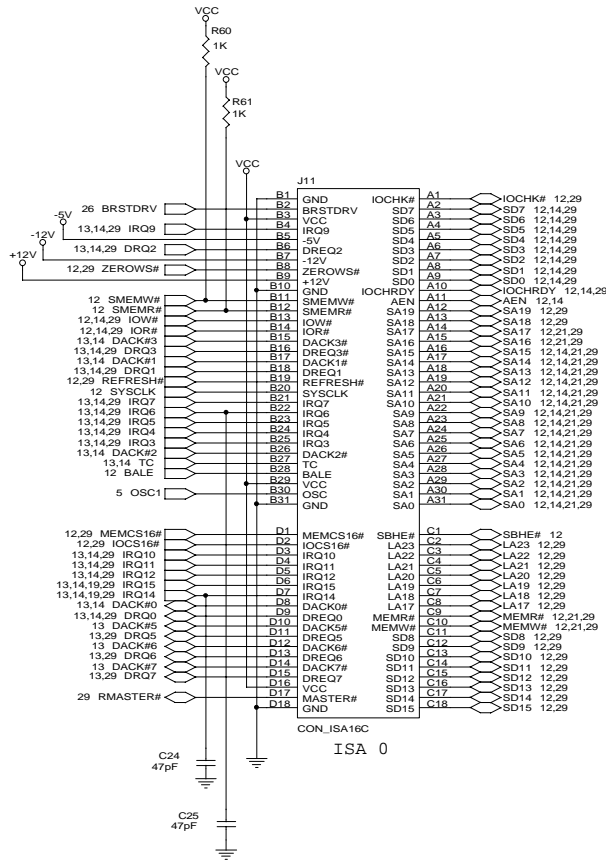


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# ISA SLOTS



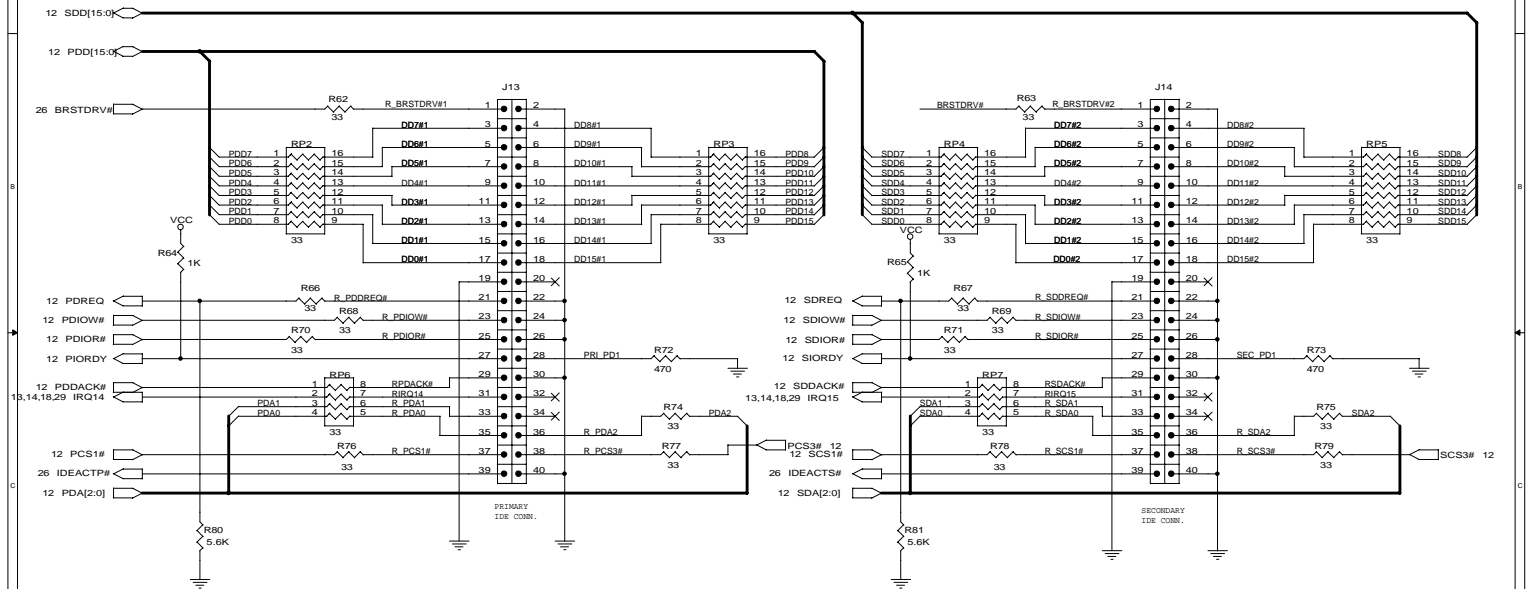
NOTE :  
 DEFAULT NO STUFF.  
 THIS CAP USED  
 TO FILTER NOISE  
 ON TC SIGNAL.

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# IDE CONNECTORS



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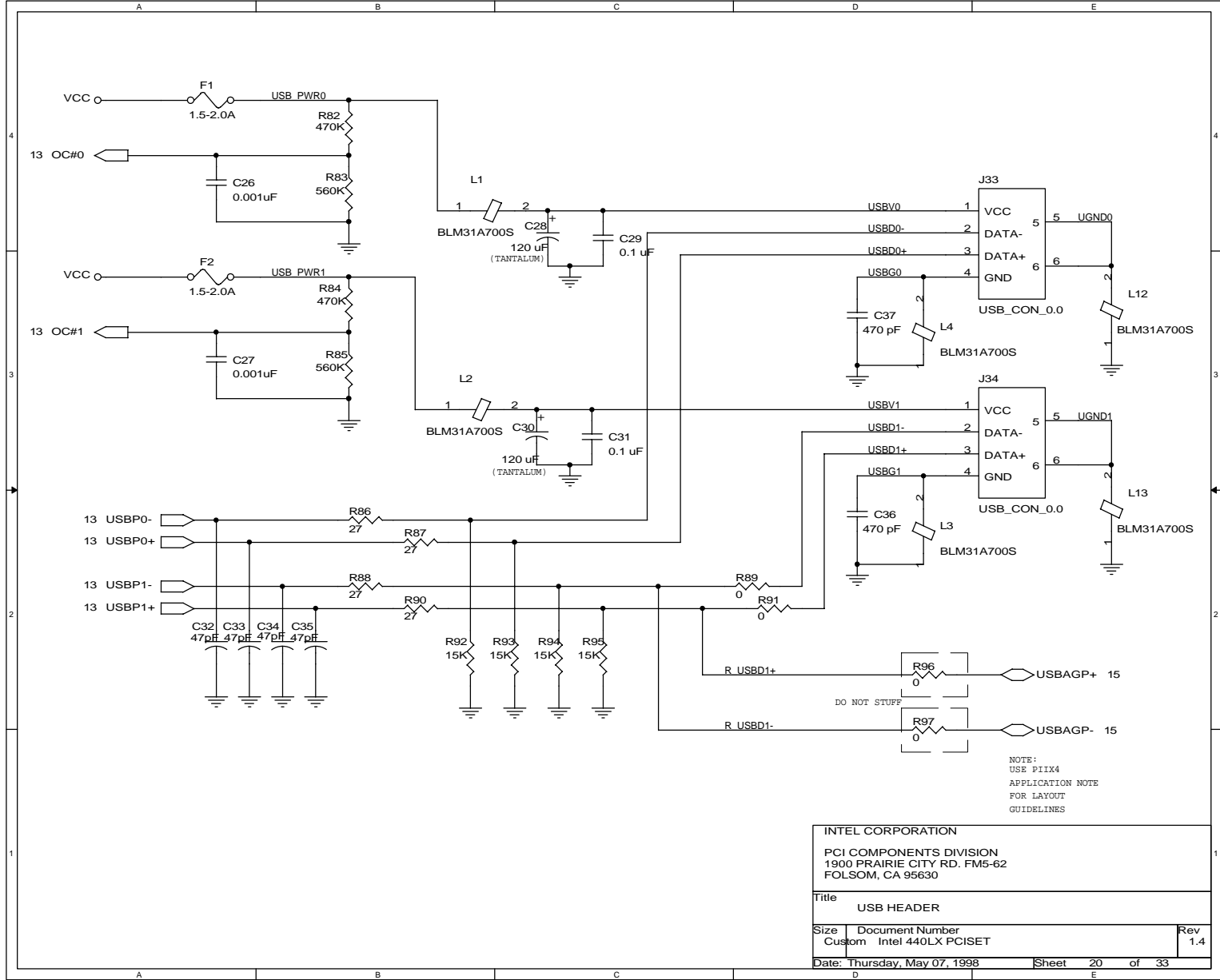
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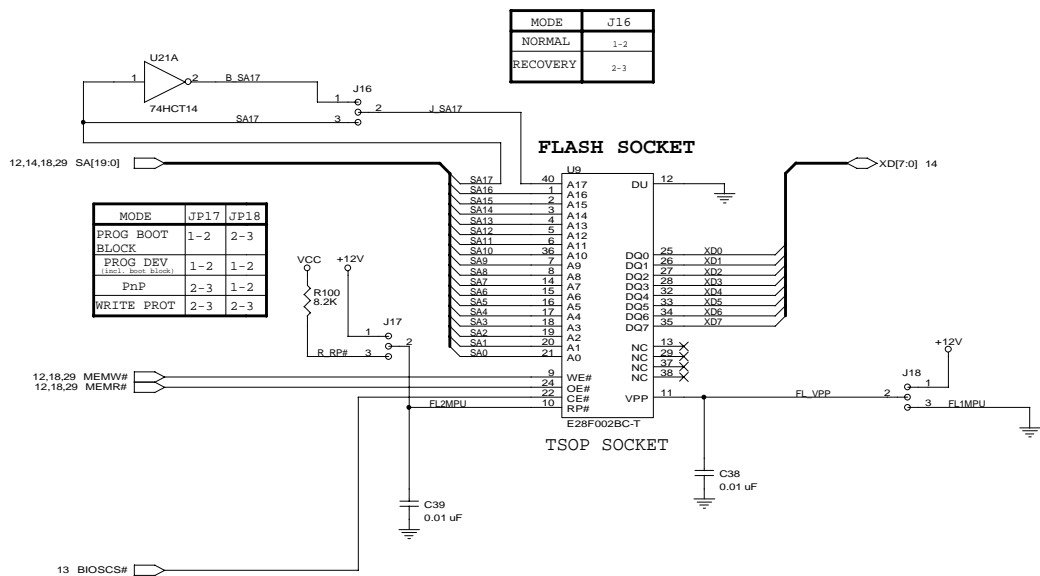
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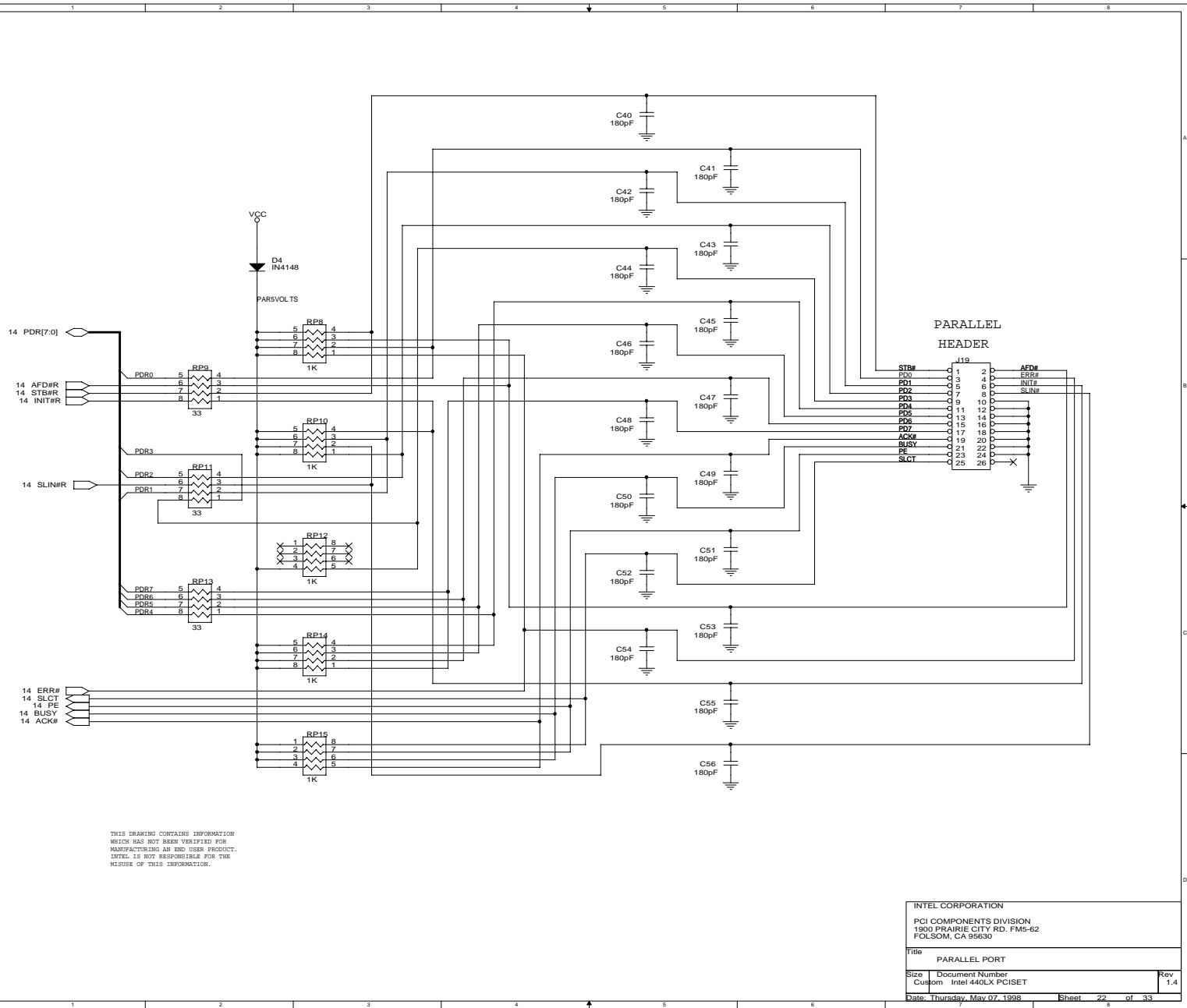
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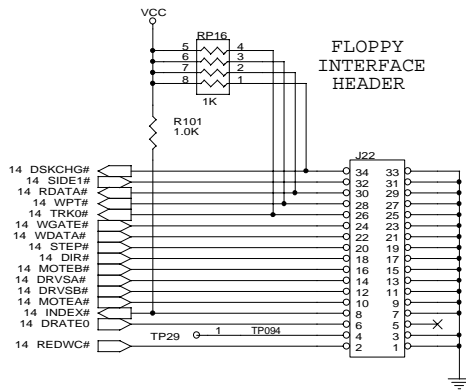
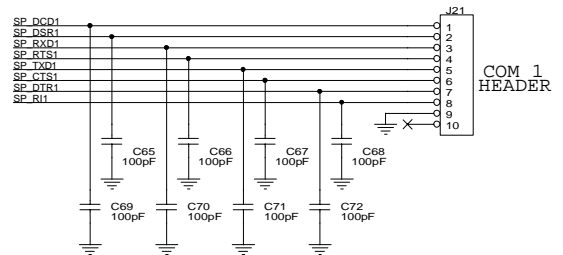
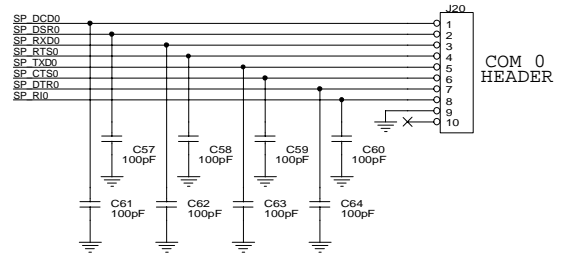
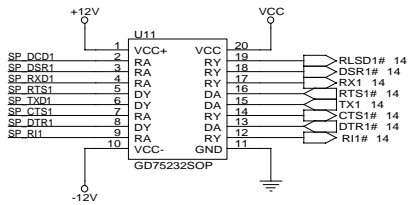
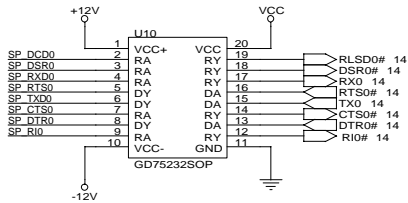
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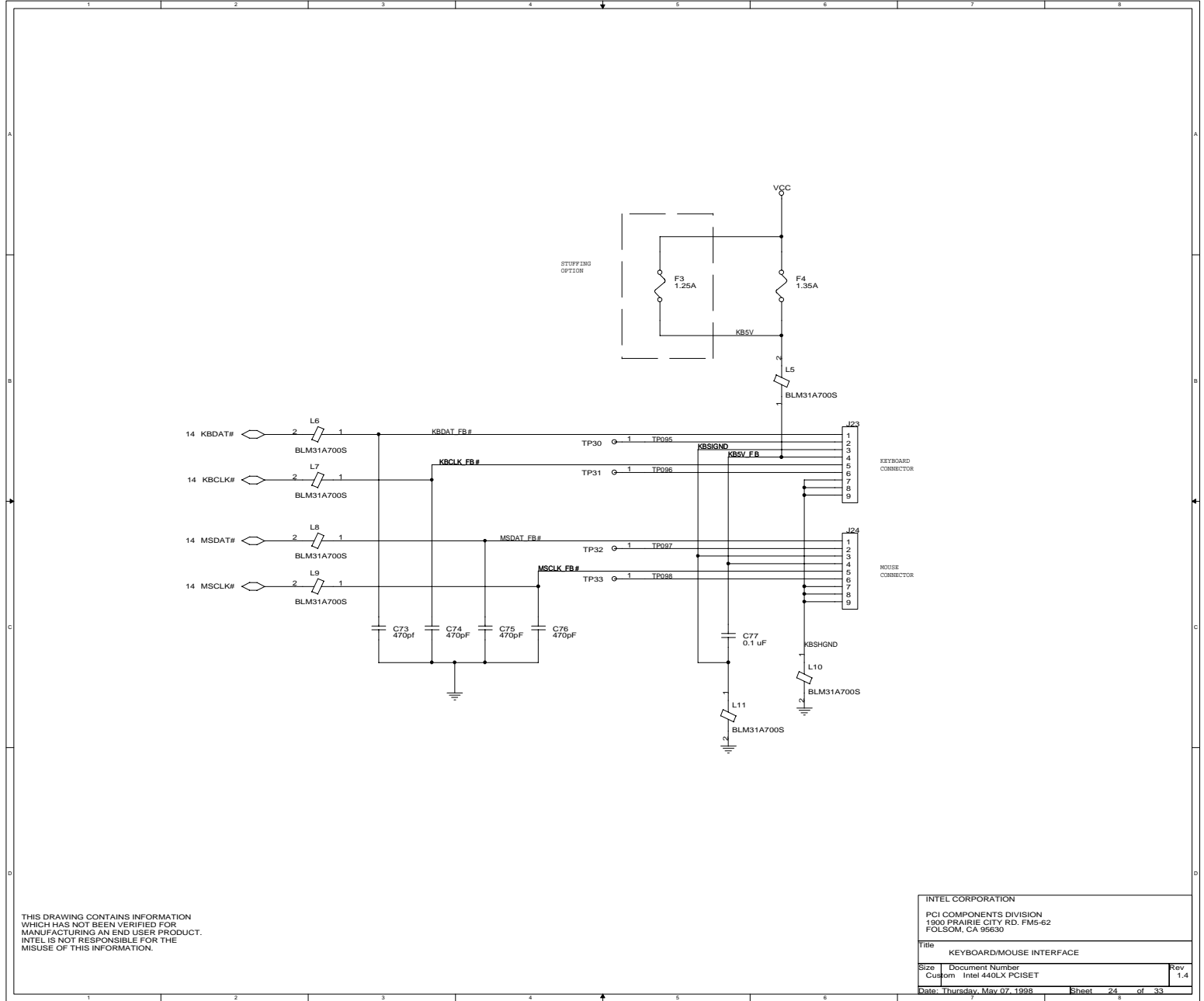
SYSTEM ROM







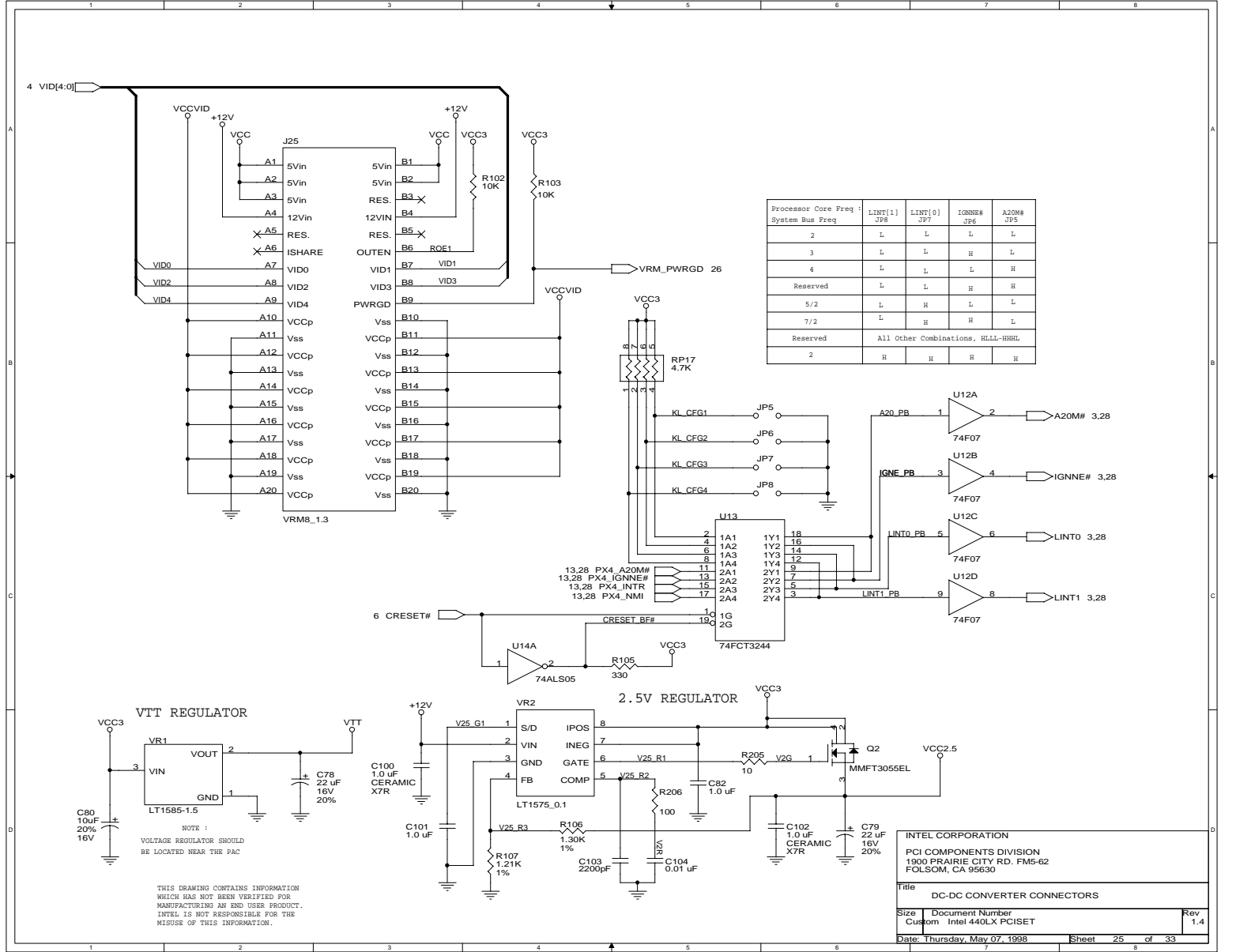
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SERIAL AND FLOPPY		
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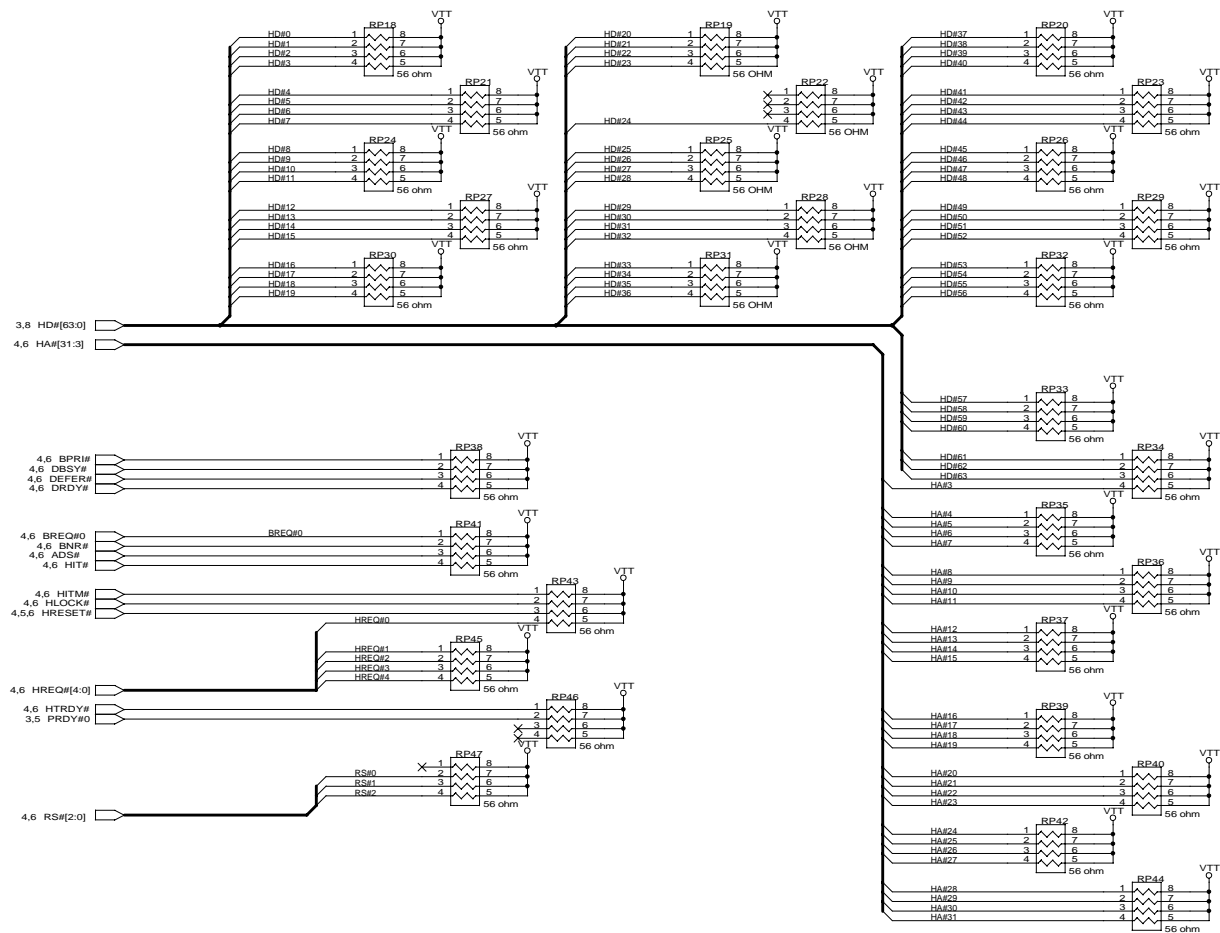
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# GTL+ TERMINATION RESISTORS



NOTE : VTT = TERMINATION VOLTAGE

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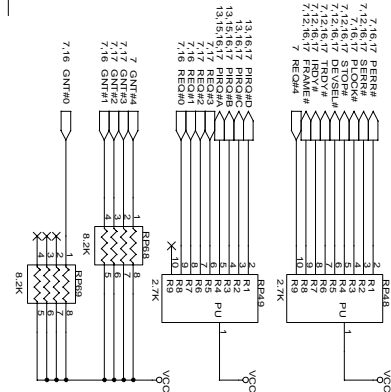
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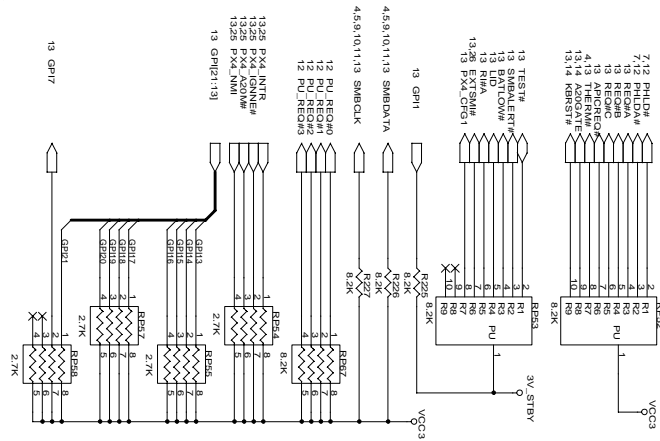
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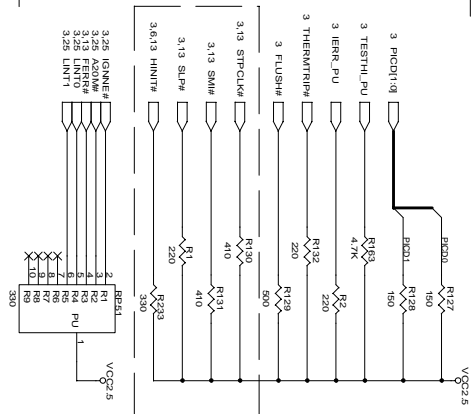
## PCI BUS



## PIIX4



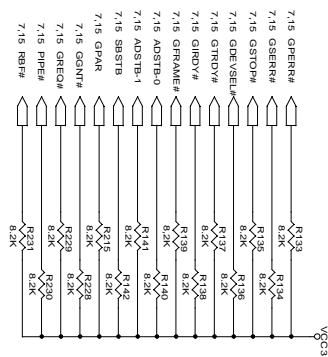
## SLOT 1



NOTE :

RESISTOR VALUES ON SIGNALS  
STCCLK#, SM1#, SLP# & HINT#  
ENABLE AN LAI TO BE USED FOR  
BOARD DEBUG. IF AN LAI WILL  
NOT BE USED FOR DEBUG THEN  
THE RESISTOR VALUES SHOULD  
BE CHANGED TO 1K OHM.

# AGP



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**ISA BUS PULLUPS**

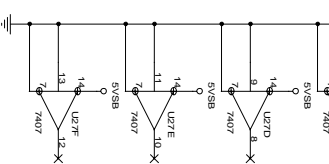
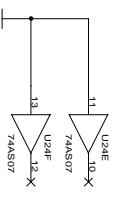
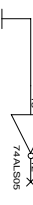
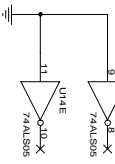
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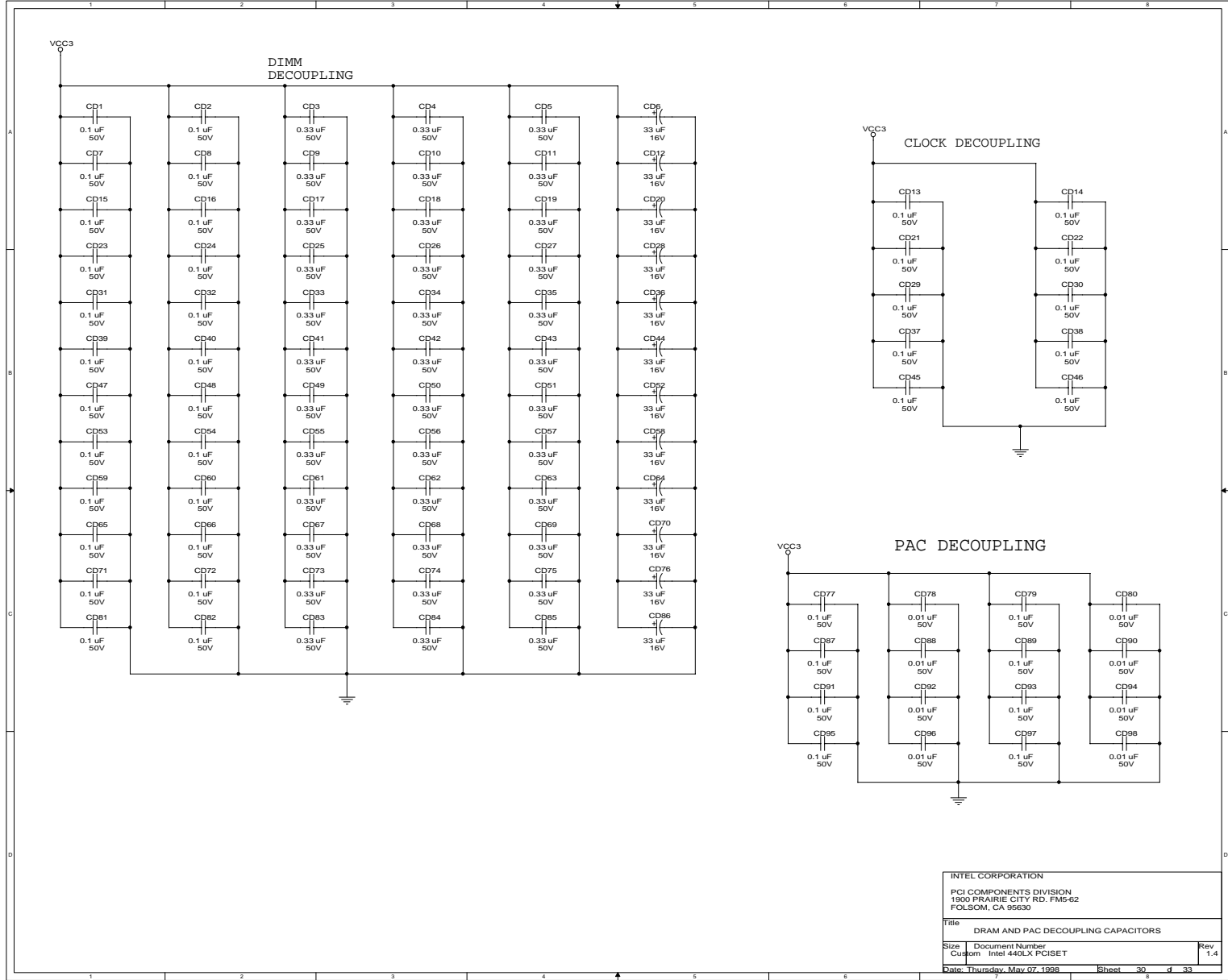
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Figure 1 is a schematic diagram of a multi-band antenna. It features a single feed line at the top left, which branches into three separate antenna structures. Each structure consists of a patch antenna with a central feed point connected to a VCC line. The patch dimensions and feed positions are labeled for each band.

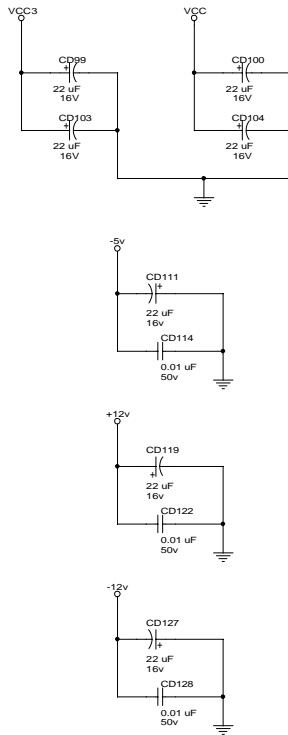
- Top Structure (12.14 GHz):** The patch is labeled with dimensions 12.14, 18.21, and 5A19.01. The feed point is labeled with dimensions 10, 10, and 10.
- Middle Structure (18.21 GHz):** The patch is labeled with dimensions 18.21, 18.21, and 18.21. The feed point is labeled with dimensions 10, 10, and 10.
- Bottom Structure (5A19.01 GHz):** The patch is labeled with dimensions 5A19.01, 5A19.01, and 5A19.01. The feed point is labeled with dimensions 10, 10, and 10.



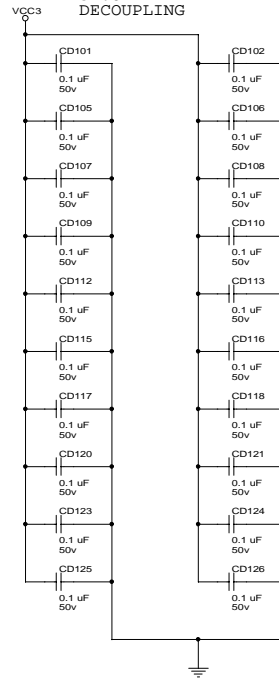


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### BULK DECOUPLING



### 3 VOLT DECOUPLING



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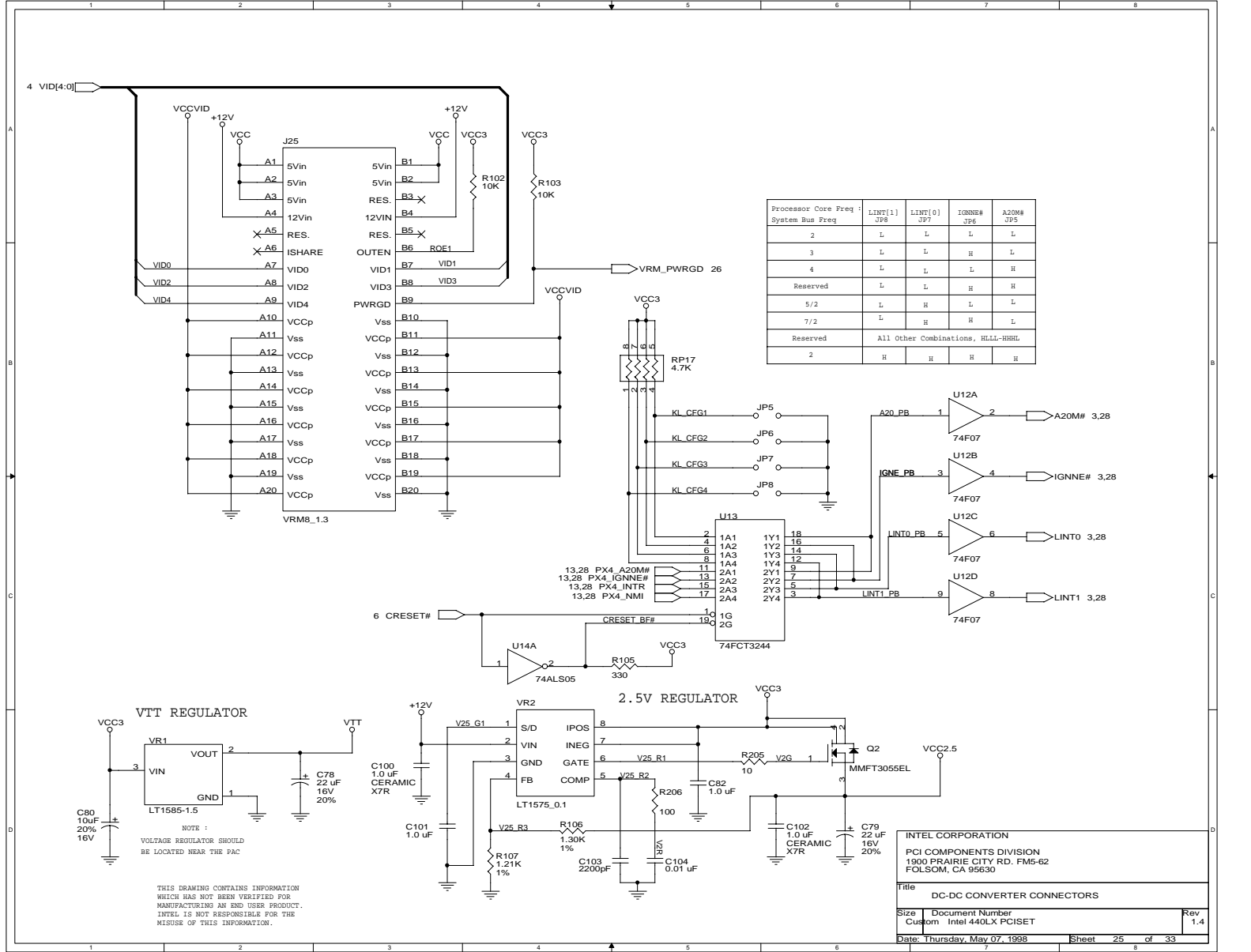
Title 3.3 VOLT AND BULK POWER DECOUPLING

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<p>REVISION 1.0 - First release of 440LX PCIset schematics.</p> <p>REVISION 1.1 - Update of Rev 1.0 440LX PCIset schematics.</p> <p>PAGE 3 : TESTHI pulled to 2.5 volts thru 220 ohms.</p> <p>PAGE 5 : Pinout of 20-pin I/O clock synthesizer device updated.</p> <p>330 ohm pullup to 2.5 volts added to PIRQ0.</p> <p>Pullups on PREQ[3:1], SMBDATA, and SMBCLK deleted.</p> <p>PG 6,7,8 : PAC ballout as of 9-26-96 used.</p> <p>CKE from PAC buffered with 74LVC245 CMOS device.</p> <p>PG 9,10,11 : MAA11 routed to DIMM SA0, MAA12 to SA1, MAA13 to A11.</p> <p>DIMM pins 31 and 44 grounded and pin 48 -&gt; WE# for EDO DIMMs.</p> <p>DIMM control signals ( WE#, SBAS#, SCAS#, RCSA#, and CDQCS# ) for DIMMs 0 and 2 swapped.</p> <p>SMBus address starts from 02H on DIMMs ( SA210 ).</p> <p>PAGE 11 : CDQAS# signals re-ordered on the pins of DIMM connector #2.</p> <p>PAGE 13 : SUSCLK pin on PIIX4 became no-connect.</p> <p>IRQ# now shown as a bi-directional signal.</p> <p>'ALS08 and '07 deleted because INIT# on PAC is now OD output.</p> <p>CONF102 pin on PIIX4 pulled to ground with 8.2K resistor.</p> <p>RCIN# name changed to KBRST# and pulled to 3.3V thru 8.2K.</p> <p>Signal A20GATE pulled to 3.3V thru 8.2K resistor.</p> <p>PAGE 14 : QSC0 clock to PIIX4 deleted due to redundancy.</p> <p>XTAL1 input pulled up to VCC through 8.2K resistor.</p> <p>KEYLOCK# input pulled up to VCC through 8.2K resistor.</p> <p>Infrared header rewired, IRRK - pin 1, IRTX - pin2.</p> <p>PAGE 15 : SMB0 &amp; SMB1 pins on AGP connector now noconnects.</p> <p>PAGE 18 : New symbol used for ISA connectors.</p> <p>PAGE 19 : Pullup on SDIOR# moved to SIORDY.</p> <p>PAGE 21 : Deleted 0 ohm resistors R98 and R99, updated jumper tables.</p> <p>FLASH changed to TSOP pinout instead of PSOP.</p> <p>PAGE 26 : Capacitor on CPU Fan header changed from 470pF to 0.1uF.</p> <p>POWEROK circuitry revised with HC14 &amp; HC32 replacing HCT14 &amp; F32 and power from 3.3V Standby.</p> <p>PAGE 27 : Swapped signals PX4_INTR and PX4_A20M# on 74VHC124 and 7407 buffers.</p> <p>PAGE 28 : Pullups on PCI control signals changed from 10K to 2.7K.</p> <p>PAGE 29 : Pullup on REFRESH# changed from 300 to 1K.</p>	<p>REVISION 1.2 - Update of Rev 1.1 440LX PCIset schematics.</p> <p>PAGE 3 : Slot 1 pin B12, UP#, now no-connect.</p> <p>PAGE 4 : Slot 1 pin B109, VCC, now no-connect.</p> <p>PAGE 5 : New CK3D pinout used for Host/DRAM/PCI clock.</p> <p>REPORT routed to XTALIN of CKIO, crystal circuit removed from CKIO XTALIN/OUT.</p> <p>10 ohm series termination added to clock outputs.</p> <p>MECCO and Freq. Sel. jumper. removed, Sel pin pulled up.</p> <p>PG 9,10,11 : DIMM SA[2:0] changed to match S.V. board for BIOS compatibility. DIMM0=2H, DIMM1=4H, DIMM2=0H.</p> <p>PAGE 12 : PIIX4 pinout modified, GP18/HCT# renamed GP18/THERM#.</p> <p>PCI REQ[3:0] routed to pullups only.</p> <p>PAGE 13 : Added 2 jumpers, 'HCT14 and 'HC32 to A20M# from PIIX4.</p> <p>Schottky diodes converted to dual Schottky diodes.</p> <p>Renamed IDE interface signals on the PIIX4 and IDE page.</p> <p>PAGE 14 : Added crystal and 2 caps to XTAL circuit of Ultra I/O.</p> <p>PAGE 15 : Deleted 74AS07 buffers and pullups on PIRQ#.</p> <p>SMBCLK connected to pin B66, SMBDATA to A66.</p> <p>PAGE 20 : Header broken into 2 USB connectors.</p> <p>Polarity symbols added to polarized caps.</p> <p>PAGE 25 : UP# now no-connect on Slot1, pulled up on VRM.</p> <p>PAGE 26 : External SMI jumper and circuit deleted (jumper, U6B 'ALS08, U12F 'F07, debounce circuit).</p> <p>PWROK circuit modified : USC.D &amp; E from 74HC14 to 74ALS05 powered by VCC, U17 (74HC12) deleted.</p> <p>R120 &amp; R124 changed to 8.1K on PWR0K circuit.</p> <p>R126 replaced with Zener diode, R123 changed from 3.48K to 410 ohm on 3V_STBY circuit.</p> <p>C91 on RSMRST# changed from 0.01uF to 1.0uF.</p> <p>RSMRST# now powered from 5VSB, added 2 'HCT14 gates and voltage divider to circuit.</p> <p>Deleted R168 &amp; C96, added 2 'HC14 gates to PWR0K from power connector.</p> <p>CPU fan header changed to 3-pin header.</p> <p>Added 0.1 uF cap for debounce to PWR_WTN circuit.</p> <p>PAGE 28 : All PCI control signals pulled through 8.2K to 3.3V.</p> <p>PIPE# and DBF# pulled to 3.3V through 8.2K.</p> <p>GP11 and PX4_CFQ1 pulled to 3V_STBY thru 8.2K.</p> <p>RP55, 57 &amp; 58 changed from 1K to 2.7K.</p> <p>PAGE 29 : IRQ12 pulled to 5.0V through 8.2K.</p> <p>Pullup on REFRESH# changed from 300 to 1K ohms.</p> <p>IRQ# now pulled to 3V_STBY thru 8.2K.</p> <p>Unused gates added to ISA pullup page.</p>	<p>REVISION 1.3 - Update of Rev 1.2 440LX PCIset schematics.</p> <p>PAGE 3 : Slot 1 pinout changed : pin B01 from RESERVED to EMI; pin B15 from FANFALA to RESERVED; pin B21 from EMI to 100/66#; pin B100 from RESERVED to EMI; pin B101 from EMI to S_O#.</p> <p>Connected signal SL# from PIIX4 to Slot 1 to support sleep state.</p> <p>PAGE 4 : Added LM75 Thermal Sensor device to THERM# and SMB bus.</p> <p>Added zero ohm resistors and jumpers to VID[4:0] for voltage select on VRM.</p> <p>Connected pin B101 to GND.</p> <p>Connected pin B109 to VCC ( 5 volts ).</p> <p>PAGE 7 : PAC pin W4 name changed from DBF# to RBP#. Signal renamed from DBF# to RBP# also.</p> <p>PG 9,10,11 : DIMM SA[2:0] changed to DIMM0=0H, DIMM1=1H, DIMM2=2H.</p> <p>PAGE 13 : Removed resistor NS1 from PIIX4 RTC crystal circuit.</p> <p>Signal GP117 named incorrectly for PIIX4 pin J19, changed to GP17 and pulled to 3.3V through 2.7K.</p> <p>Device U5 changed from 74HC14 to 74LVC14 for 3V compatibility.</p> <p>Removed UPI, route RTC_BAT direct to PIIX4, placed 0 ohm in series to SMC input. Added JP19 to clear CMOS.</p> <p>Removed GP11 &amp; 12, U21 &amp; U23, A20M# circuit not needed for 8-0 PIIX4 units.</p> <p>PAGE 14 : Added 74AS07 gate to IRQ# to convert from 5V to 3V_STBY.</p> <p>PAGE 15 : Added 74AS07 gates with 4.7K pullups to 3.3V on PIRQ# and PIRQ#B.</p> <p>Pin A66 name changed, SMB1 -&gt; SMBDATA, B66 name changed, SMB0 -&gt; SMBCLK.</p> <p>PAGE 16,17 : Added pullups to SBO, SDONE, TMS &amp; TDT, pulldowns to TRST# &amp; TCK to comply with PCI 2.1 Spec.</p> <p>Changed PCI connector IDSELs from AD28 - 31 to AD26, AD27, AD29, AD31.</p> <p>PAGE 25 : Changed 2.5V generation from LT1587 to LT1575 plus power FET and associated circuit.</p> <p>VRM# pinout changed, pin B5 from UP# to RESERVED. Pullup R104 deleted.</p> <p>PAGE 26 : Removed voltage divider resistors R120, 124, 201 &amp; 202 on RSMRST# and PWR0K.</p> <p>Replaced three 74ALS05 gates wire-ored with 74HC10 and 74P07 on POWERGOOD circuit.</p> <p>Device U5 changed from 74HC14 to 74LVC14, RSMRST# powered by 3V_STBY.</p> <p>R123 changed from 410 to 56 ohm on 3V_STBY.</p> <p>R125 changed from 1K to 22K on RSMRST#.</p> <p>PAGE 28 : PCI control pullups changed to 2.7K -&gt; 5V from 8.2K -&gt; 3.3V. GNTX still pulled to 3.3V thru 8.2K.</p> <p>GPAP pulled to 3.3V through 8.2K per DCN #70.</p> <p>RP56 broken into discrete resistors for AGP layout considerations. R133 - R138 converted from 10K to 8.2K.</p> <p>RP66 broken into discrete resistors. SMBDATA and SMBCLK pulled to 3.3V thru 8.2K.</p> <p>PAGE 29 : R-Pack added to pull IRQ1 to VCC thru 8.2K.</p> <p>Pullup on ZEROWS#, MEMCS16# &amp; IOCS16# changed from 300 ohm to 1K.</p>	<p>REVISION 1.4 - Update of Rev 1.3 440LX PCIset schematics.</p> <p>PAGE 3 : Pullups on SLP#, IERR# and TESTHI moved to Page 28.</p> <p>PAGE 4 : VID[4:0] jumpers pulled to VCC instead of VCC3.</p> <p>PAGE 5 : Series termination changed from 10 ohms to 22 ohms on SDRAM-I/O clocks and 33 ohms on all other clocks.</p> <p>PAGE 6 : VCCA pin R3 renamed VCC. AGND pin R5 renamed GND. VCC pins AD12 &amp; R4 added to list of VCC pins on part.</p> <p>JP2 changed to 3-pin jumper. Pulldown R236 added to config PAC with IOQD = MAX.</p> <p>PG 9,10,11 : PCIRST routed through U14, 74ALS05 to OR pins on all DIMM modules to disable MECC[7:0] output during board reset.</p> <p>PAGE 13 : Added R234 &amp; R235 to PIIX4 RTC crystal inputs.</p> <p>GPIO connected to signal FAN_ON instead of TP1.</p> <p>PAGE 15 : SMBDATA &amp; SMBCLK no longer routed to AGP connector.</p> <p>PAGE 26 : Circuitry on signals PWRBT#, PWR0K, RSMRST# and FAN_ON modified and converted from 3V_STBY to 5VSB.</p> <p>PAGE 28 : Added pullups for SLP#, IERR# and TESTHI. Added note about resistor changes for LA1 use.</p> <p>PAGE 29 : Added unused 74AS07 gates.</p>
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